THIS DOCUMENT HAS NOT BEEN REGISTERED BY THE SECURITIES COMMISSION MALAYSIA ("SC"). THE INFORMATION IN THIS DOCUMENT MAY BE SUBJECT TO FURTHER AMENDMENTS BEFORE BEING REGISTERED BY THE SC. UNDER NO CIRCUMSTANCES SHALL THIS DOCUMENT CONSTITUTE AN OFFER FOR SUBSCRIPTION OR PURCHASE OF, OR AN INVITATION TO SUBSCRIBE FOR OR PURCHASE THE SECURITIES.

PROSPECTUS

SKYECHIP
Accelerating Computing

SKYECHIP BERHAD
(Registration No. 201901014484 (1323812-D))
(Incorporated in Malaysia under the Companies Act 2016)

INITIAL PUBLIC OFFERING ("IPO") OF 400,000,000 ORDINARY SHARES IN SKYECHIP BERHAD ("SKYECHIP" OR "COMPANY") ("IPO SHARES") IN CONJUNCTION WITH THE LISTING OF AND QUOTATION FOR THE ENTIRE ENLARGED ISSUED ORDINARY SHARES IN SKYECHIP ("SKYECHIP SHARES" OR "SHARES") ON THE MAIN MARKET OF BURSA MALAYSIA SECURITIES BERHAD COMPRISING A PUBLIC ISSUE OF 400,000,000 NEW SHARES INVOLVING:

(I) INSTITUTIONAL OFFERING OF 264,672,800 IPO SHARES TO INSTITUTIONAL AND SELECTED INVESTORS AT THE INSTITUTIONAL PRICE TO BE DETERMINED BY WAY OF BOOKBUILDING ("INSTITUTIONAL PRICE"); AND

(II) RETAIL OFFERING OF 135,327,200 IPO SHARES TO THE DIRECTORS OF SKYECHIP, ELIGIBLE EMPLOYEES OF SKYECHIP AND ITS SUBSIDIARIES ("GROUP"), PERSONS WHO HAVE CONTRIBUTED TO THE SUCCESS OF THE GROUP AND THE MALAYSIAN PUBLIC AT THE RETAIL PRICE OF RM[●] PER IPO SHARE ("RETAIL PRICE"), PAYABLE IN FULL UPON APPLICATION AND SUBJECT TO REFUND OF THE DIFFERENCE BETWEEN THE RETAIL PRICE AND THE FINAL RETAIL PRICE (AS DEFINED IN THIS PROSPECTUS) IN THE EVENT THAT THE FINAL RETAIL PRICE IS LESS THAN THE RETAIL PRICE,

SUBJECT TO THE CLAWBACK AND REALLOCATION PROVISIONS.

THE FINAL RETAIL PRICE WILL BE EQUAL TO THE LOWER OF:

(A) THE RETAIL PRICE; OR

(B) THE INSTITUTIONAL PRICE.

Principal Adviser, Lead Bookrunner, Joint Bookrunner, Managing Underwriter and Joint Underwriter

Maybank
Investment Bank

Maybank Investment Bank Berhad
(Company Registration No. 197301002412)
(A Participating Organisation of Bursa Malaysia Securities Berhad)

Joint Bookrunner and Joint Underwriter

CIMB

CIMB Investment Bank Berhad
(Registration No. 197401001266 (18417-M))

NO SECURITIES WILL BE ALLOTTED OR ISSUED BASED ON THIS PROSPECTUS AFTER SIX MONTHS FROM THE DATE OF THIS PROSPECTUS.

[THE SC HAS APPROVED OUR IPO UNDER SECTION 214(1) OF THE CAPITAL MARKETS AND SERVICES ACT 2007.]

THIS PROSPECTUS [HAS BEEN REGISTERED] BY THE SC. THE APPROVAL OF OUR IPO AND REGISTRATION OF THIS PROSPECTUS, SHOULD NOT BE TAKEN TO INDICATE THAT THE SC RECOMMENDS OUR IPO OR ASSUMES RESPONSIBILITY FOR THE CORRECTNESS OF ANY STATEMENT MADE, OPINION EXPRESSED OR REPORT CONTAINED IN THIS PROSPECTUS. THE SC HAS NOT, IN ANY WAY, CONSIDERED THE MERITS OF OUR SHARES BEING OFFERED FOR INVESTMENT.

THE SC IS NOT LIABLE FOR ANY NON-DISCLOSURE ON THE PART OF OUR COMPANY AND TAKES NO RESPONSIBILITY FOR THE CONTENTS OF THIS PROSPECTUS, MAKES NO REPRESENTATION AS TO ITS ACCURACY OR COMPLETENESS, AND EXPRESSLY DISCLAIMS ANY LIABILITY FOR ANY LOSS THAT YOU MAY SUFFER ARISING FROM OR IN RELIANCE UPON THE WHOLE OR ANY PART OF THE CONTENTS OF THIS PROSPECTUS.

INVESTORS ARE ADVISED TO READ AND UNDERSTAND THE CONTENTS OF THIS PROSPECTUS. IF IN DOUBT, PLEASE CONSULT A PROFESSIONAL ADVISER.

FOR INFORMATION CONCERNING RISK FACTORS WHICH SHOULD BE CONSIDERED BY PROSPECTIVE INVESTORS, SEE "RISK FACTORS" COMMENCING ON PAGE 41.

LISTING SOUGHT: MAIN MARKET OF BURSA MALAYSIA SECURITIES BERHAD

THIS PROSPECTUS IS NOT TO BE DISTRIBUTED OUTSIDE MALAYSIA

THIS PROSPECTUS IS DATED [●]

All defined terms used in this Prospectus are defined under "Presentation of Financial and Other Information" commencing on page viii, "Definitions" commencing on page xii and "Glossary of Technical Terms" commencing on page xx.

RESPONSIBILITY STATEMENTS

Our Directors and our Promoters have seen and approved this Prospectus. They collectively and individually accept full responsibility for the accuracy of the information. Having made all reasonable enquiries, and to the best of their knowledge and belief, they confirm that there is no false or misleading statement or other facts which if omitted, would make any statement in this Prospectus false or misleading.

Maybank IB, being the Principal Adviser, Lead Bookrunner and Joint Bookrunner for the Institutional Offering and Managing Underwriter and Joint Underwriter for the Retail Offering, acknowledges that, based on all available information, and to the best of its knowledge and belief, this Prospectus constitutes a full and true disclosure of all material facts concerning our IPO.

It is to be noted that the role of CIMB IB in our IPO is limited to being the Joint Bookrunner for the Institutional Offering and Joint Underwriter for the Retail Offering.

STATEMENTS OF DISCLAIMER

[Our Company has obtained the approval of Bursa Securities for our Listing.] Admission to the Official List of Bursa Securities is not to be taken as an indication of the merits of our IPO, our Company or our Shares.

[This Prospectus, together with the Application Forms, have also been lodged with the ROC,] who takes no responsibility for its contents.

OTHER STATEMENTS

Investors should note that they may seek recourse under Sections 248, 249 and 357 of the CMSA for breaches of securities laws including any statement in this Prospectus that is false, misleading, or from which there is a material omission, or for any misleading or deceptive act in relation to this Prospectus or the conduct of any other person in relation to our Company.

Our Shares are offered to the public on the premise of full and accurate disclosure of all material information concerning our IPO, for which any person set out in Section 236 of the CMSA, is responsible.

[Our Shares are classified as Shariah-compliant by the SAC. This classification remains valid from the date of issue of this Prospectus until the next Shariah compliance review undertaken by the SAC. The new status is released in the updated list of Shariah-compliant securities, on the last Friday of May and November.]

Investors should not take the agreement by the Managing Underwriter and Joint Underwriters named in this Prospectus to underwrite our Shares under the Retail Offering as an indication of the merits of our Shares being offered.

This Prospectus is published solely in connection with our IPO. Our Shares are being offered solely in Malaysia on the basis of the information contained and representations made in this Prospectus. Our Company, our Promoters, the Principal Adviser, Lead Bookrunner, Joint Bookrunners, Managing Underwriter and Joint Underwriters have not authorised anyone to provide any information or to make any representation not contained in this Prospectus. Any information or representation not contained in this Prospectus must not be relied upon as having been authorised by our Company, our Promoters, the Principal Adviser, Lead Bookrunner, Joint Bookrunners, Managing Underwriter and Joint Underwriters or any of their respective directors, or any other persons involved in our IPO.

The distribution of this Prospectus and our IPO are subject to the laws of Malaysia. This Prospectus has not been and will not be made to comply with the laws of any jurisdiction other than Malaysia, and has not been and will not be lodged, registered or approved pursuant to any applicable securities or equivalent legislation or by any regulatory authority or other relevant body of any jurisdiction other than Malaysia. Accordingly, this Prospectus may not be used for the purpose of and does not constitute an offer for subscription or purchase or invitation to subscribe for or purchase of our Shares in any jurisdiction or in any circumstance in which such an offer is not authorised or is unlawful or to any person to whom it is unlawful to make such offer or invitation. The distribution of this Prospectus and the offering of our Shares in certain other jurisdictions may be restricted by law. Prospective investors who may be in possession of this Prospectus are required to inform themselves and to observe applicable restrictions.

We will not, prior to acting on any acceptance in respect of our IPO, make or be bound to make any enquiry as to whether you have a registered address in Malaysia and will not be deemed to accept any liability whether or not any enquiry or investigation is made in connection to it. We will further assume that you have accepted our IPO in Malaysia and will be subject to the laws of Malaysia in connection to it.

It will be your sole responsibility to ensure that your application for our IPO is in compliance with the terms of our IPO and will not be in contravention of any laws of countries or jurisdictions other than Malaysia to which you may be subjected to. It will also be your sole responsibility to consult your legal and/or other professional adviser on the laws to which our IPO or you are or might be subjected to. Neither we nor our Promoters, the Principal Adviser, Lead Bookrunner, Joint Bookrunners, Managing Underwriter and Joint Underwriters nor any other advisers in relation to our IPO will accept any responsibility or liability in the event that any application made by you shall become illegal, unenforceable, avoidable or void in any country or jurisdiction.

However, we reserve the right, in our absolute discretion, to treat any acceptance as invalid if we believe that such acceptance may violate any law or applicable legal or regulatory requirements.

ELECTRONIC PROSPECTUS/INTERNET SHARE APPLICATION

This Prospectus can also be viewed or downloaded from Bursa Securities' website at www.bursamalaysia.com. The contents of the Electronic Prospectus and the copy of this Prospectus registered with the SC are the same.

The internet is not a fully secure medium. Your Internet Share Application may be subject to risks of data transmission, computer security threats such as viruses, hackers and crackers, faults with computer software and other events beyond the control of the Internet Participating Financial Institutions or Participating Securities Firms. These risks cannot be borne by the Internet Participating Financial Institutions or Participating Securities Firms.

If you doubt the validity or integrity of the Electronic Prospectus, you should immediately request a paper/printed copy of this Prospectus from us or the Issuing House. If there is any discrepancy between the contents of the Electronic Prospectus and the contents of the paper/printed copy of this Prospectus, the contents of the paper/printed copy of this Prospectus which are identical to the copy of the Prospectus registered with the SC shall prevail.

In relation to any reference in this Prospectus to third party internet sites ("**Third-Party Internet Sites**"), whether by way of hyperlinks or by way of description of the Third-Party Internet Sites, you acknowledge and agree that:

(i) we do not endorse and are not affiliated in any way to the Third-Party Internet Sites. Accordingly, we are not responsible for the availability of, or the content or any data, information, file or other material provided on the Third-Party Internet Sites. You bear all risks associated with the access to or use of the Third-Party Internet Sites;

(ii) we are not responsible for the quality of products or services in the Third-Party Internet Sites, particularly in fulfilling any of the terms of your agreements with the Third-Party Internet Sites. We are also not responsible for any loss or damage or cost that you may suffer or incur in connection with or as a result of dealing with the Third-Party Internet Sites or the use of or reliance on any data, information, file or other material provided by the Third-Party Internet Sites; and

(iii) any data, information, file or other material downloaded from the Third-Party Internet Sites is done at your own discretion and risk. We are not responsible, liable or under obligation for any damage to your computer system or loss of data resulting from the downloading of any such data, information, file or other material.

Where an Electronic Prospectus is hosted on the website of the Internet Participating Financial Institution or Participating Securities Firm, you are advised that:

(i) the Internet Participating Financial Institution or Participating Securities Firm is only liable in respect of the integrity of the contents of the Electronic Prospectus, to the extent of the contents of the Electronic Prospectus on the web server of the Internet Participating Financial Institution or Participating Securities Firm which may be viewed via your web browser or other relevant software. The Internet Participating Financial Institution or Participating Securities Firm is not responsible for the integrity of the contents of the Electronic Prospectus which has been obtained from the web server of the Internet Participating Financial Institution or Participating Securities Firm and subsequently communicated or disseminated in any manner to you or other parties;

(ii) while all reasonable measures have been taken to ensure the accuracy and reliability of the information provided in the Electronic Prospectus, the accuracy and reliability of the Electronic Prospectus cannot be guaranteed because the internet is not a fully secure medium; and

(iii) the Internet Participating Financial Institution or Participating Securities Firm is not liable (whether in tort or contract or otherwise) for any loss, damage or costs that you or any other person may suffer or incur due to, as a consequence of or in connection with any inaccuracies, changes, alterations, deletions or omissions in respect of the information provided in the Electronic Prospectus which may arise in connection with or as a result of any fault with web browsers or other relevant software, any fault on your or any third party's personal computer, operating system or other software, viruses or other security threats, unauthorised access to information or systems in relation to the website of the Internet Participating Financial Institution or Participating Securities Firm, and/or problems occurring during data transmission which may result in inaccurate or incomplete copies of information being downloaded or displayed on your personal computer.

INDICATIVE TIMETABLE

The following events are intended to take place on the following indicative time and/or date:

Event	Time and/or date
Opening of the Institutional Offering(1)	[●]
Issuance of the Prospectus/Opening of the Retail Offering	10.00 a.m., [●]
Closing of the Retail Offering	5.00 p.m., [●]
Closing of the Institutional Offering	[●]
Price Determination Date	[●]
Balloting of applications for our IPO Shares under the Retail Offering	[●]
Allotment of our IPO Shares to successful applicants	[●]
Listing	[●]

Note:

(1) *Other than the Institutional Offering to the Cornerstone Investors. The Master Cornerstone Placement Agreement for the subscription of our IPO Shares by the Cornerstone Investors was entered into on [●].*

In the event there is any change to the timetable, we will advertise the notice of changes in widely circulated English and Bahasa Malaysia daily newspapers in Malaysia and make an announcement on the website of Bursa Securities.

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PRESENTATION OF FINANCIAL AND OTHER INFORMATION

All references to "SkyeChip" or "our Company" are to SkyeChip Berhad. All references to "SkyeChip Group" or "our Group" are to our Company and our subsidiaries taken as a whole. All references to "we", "us", "our" and "ourselves" are to our Company and where the context otherwise requires, our Group.

All references to the "Promoters" are to Dato' Fong Swee Kiang and Teh Chee Hak.

All references to "you" are to our prospective investors.

Certain numbers presented in this Prospectus have been rounded off to the nearest hundredth or one (1) decimal place. Any discrepancies in the tables between the amounts listed and the totals in this Prospectus are due to rounding adjustments.

Other abbreviations and acronyms used in this Prospectus are defined in the "Definitions" section and technical terms used in this Prospectus are defined in the "Glossary of Technical Terms" section. Words denoting the singular will, where applicable, include the plural and *vice versa* and words denoting the masculine gender will, where applicable, include the feminine and/or neuter gender and *vice versa*. Reference to persons will, where applicable, include companies and corporations.

Any reference to provisions of the statutes, rules, regulations, enactments or rules of stock exchange shall (where the context admits), be construed as a reference to provisions of such statutes, rules, regulations, enactments or rules of the stock exchange (as the case may be) as modified by any written law or (if applicable) amendments or re-enactments to the statutes, rules, regulations, enactments or rules of stock exchange for the time being in force.

Any reference to a time or date shall be a reference to a time or date in Malaysia, unless otherwise stated.

Any reference to the "LPD" in this Prospectus is to 19 September 2025, being the latest practicable date prior to the registration of this Prospectus with the SC.

The information on our website or any website, directly or indirectly, linked to our website does not form part of this Prospectus and you should not rely on those information for the purposes of your decision whether or not to invest in our Shares.

This Prospectus includes statistical data provided by us and various third parties and cites third-party projections regarding the growth and performance of the industry in which we operate and our estimated market share. This data is taken or derived from information published by industry sources and from our internal data. In each of such case, the source is stated in this Prospectus, provided that where no source is stated, it can be assumed that the information originates from us or is extracted from the IMR Report as included in Section 8 of this Prospectus. We have appointed Vital Factor to provide an independent market and industry review. In compiling its data for the review, Vital Factor had relied on its research methodology, industry sources, published materials, its private databanks and direct contacts within the industry.

Further, third-party projections cited in this Prospectus are subject to significant uncertainties that could cause actual data to differ materially from the projected figures. We cannot give any assurance that the projected figures will be achieved and you should not place undue reliance on the statistical data and third-party projections cited in this Prospectus.

For the purpose of this Prospectus, EBITDA is calculated as our profit for the relevant financial year plus (i) tax expense; (ii) finance costs; (iii) depreciation and amortisation, less (iv) interest income.

PRESENTATION OF FINANCIAL AND OTHER INFORMATION *(Cont'd)*

EBITDA and the related ratios presented in this Prospectus are supplemental measures of our performance and liquidity that are not required by or presented in accordance with the IFRS and MFRS. Furthermore, EBITDA is not a measure of our financial performance or liquidity under the IFRS and MFRS and should not be considered as an alternative to net income, operating income or any other performance measures derived in accordance with the IFRS or MFRS or as an alternative to cash flows from operating activities or as a measure of liquidity. In addition, EBITDA is not a standardised term, and hence, a direct comparison of EBITDA between companies may not be possible. Other companies may calculate EBITDA differently from us, limiting its usefulness as a comparative measure.

We believe that EBITDA may facilitate comparisons of operating performance from period to period and company to company by eliminating potential differences caused by variations in capital structures (affecting interest expense and finance charges), tax positions (such as the impact on periods or companies of changes in effective tax rates or net operating losses), and the age and booked depreciation and amortisation of assets (affecting relative depreciation and amortisation expenses). EBITDA has been presented because we believe that it is frequently used by securities analysts, investors and other interested parties in evaluating similar companies, many of whom present such non-IFRS and non-MFRS financial measures when reporting their results. Finally, EBITDA is presented as a supplemental measure of our ability to service debt. Nevertheless, EBITDA has limitations as an analytical tool, and prospective investors should not consider it in isolation from or as a substitute for analysis of our financial condition or results of operations, as reported under the IFRS and MFRS. Due to these limitations, EBITDA should not be considered as a measure of discretionary cash available to invest in the growth of our business.

FORWARD-LOOKING STATEMENTS

This Prospectus contains forward-looking statements. All statements, other than statements of historical facts included in this Prospectus, including, without limitation, those regarding our financial position, strategies and prospects are forward-looking statements. Such forward-looking statements involve known and unknown risks, uncertainties and other factors, which may cause our actual results, performance or achievements, or industry results, to be materially different from any future results, performance or achievements, or industry results expressed or implied by such forward-looking statements. Such forward-looking statements are based on numerous assumptions regarding our present and future strategies and the environment in which we will operate in the future. Such forward-looking statements reflect our current view with respect to future events and are not a guarantee of future performance.

Forward-looking statements can be identified by the use of forward-looking terminology such as the words "may", "will", "would", "could", "believe", "expect", "anticipate", "intend", "estimate", "aim", "plan", "forecast" or similar expressions and include all statements that are not historical facts. Such forward-looking statements include, without limitation, statements relating to:

(i) our strategies and potential growth opportunities;

(ii) our future plans and objectives;

(iii) our future financial position, earnings, cash flows and liquidity;

(iv) the demand for our products and services, trends and competitive position; and

(v) the changes to the regulatory environment in the industry and markets in which we operate.

Our actual results may differ materially from information contained in such forward-looking statements as a result of a number of factors beyond our control, including, without limitation:

(i) activities and financial position of our customers, suppliers and business partners;

(ii) general economic, business, social, political and investment environment in Malaysia and in countries where we operate or source our products and globally;

(iii) interest rates, tax rates, finance costs and exchange rates;

(iv) competitive environment in the industry in which we operate;

(v) reliance on approvals, permits and licences;

(vi) fixed and contingent obligations and commitments;

(vii) changes in accounting standards and policies;

(viii) continued availability of capital and financing;

(ix) delays or problems with the execution of our expansion plans;

(x) future regulatory or government policy changes affecting us or countries from where we operate or source our products; and

(xi) other factors beyond our control.

FORWARD-LOOKING STATEMENTS *(Cont'd)*

Additional factors that could cause actual results, performance or achievements to differ materially include, but are not limited to, those discussed in Section 5 of this Prospectus on "Risk Factors" and Section 12.2 of this Prospectus on "Management's Discussion and Analysis of Financial Condition and Results of Operations". We cannot give any assurance that the forward-looking statements made in this Prospectus will be realised. Such forward-looking statements are made only as at the LPD.

In light of these uncertainties, the inclusion of such forward-looking statements should not be regarded as a representation or warranty by us or our advisers that such plans and objectives will be achieved.

Should we become aware of any subsequent material change or development affecting a matter disclosed in this Prospectus arising from the date of registration of this Prospectus but before the date of allotment of our IPO Shares, we will further issue a supplemental or replacement prospectus, as the case may be, in accordance with the provisions of Section 238(1) of the CMSA and Paragraph 1.02, Chapter 1 of Part II (Division 6 on Supplementary and Replacement Prospectus) of the Prospectus Guidelines.

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DEFINITIONS

The following terms shall apply throughout this Prospectus unless the term is defined otherwise or the context requires otherwise:

Act	:	Companies Act 2016 of Malaysia
ADA	:	Authorised Depository Agent
Admission	:	Admission of our Shares to the Official List of the Main Market of Bursa Securities
AGM	:	Annual general meeting
Application	:	Application for our IPO Shares by way of Application Form, Electronic Share Application or Internet Share Application
Application Form(s)	:	Application form for the application of our IPO Shares under the Retail Offering accompanying this Prospectus
Areca	:	Collectively, DG 12 and ASIF 15, being funds managed by Areca Capital
Areca Capital	:	Areca Capital Sdn Bhd
ASIF 15	:	Areca Strategic Income Fund 15
ASP	:	Average selling price
ATM	:	Automated teller machine
Auditors or Reporting Accountants	:	Grant Thornton Malaysia PLT
Authorised Financial Institution	:	Authorised financial institution participating in the Internet Share Application in respect of the payment for our IPO Shares
BNM	:	Bank Negara Malaysia
Board	:	Board of Directors of our Company
Bumiputera	:	In context of: (i) individuals - Malay and the aborigines and the natives of Sabah and Sarawak as specified in the Federal Constitution of Malaysia; (ii) companies - companies which fulfil, among others, the following criteria or such other criteria as may be imposed by the MITI: (a) registered under the Act as a private company; (b) its shareholders are 100% Bumiputera; and (c) its board of directors (including its staff) are at least 51% Bumiputera; and (iii) cooperatives - cooperatives whose shareholders or cooperative members are at least 95% Bumiputera or such other criteria as may be imposed by the MITI
Bursa Depository	:	Bursa Malaysia Depository Sdn Bhd

DEFINITIONS *(Cont'd)*

Bursa Securities	:	Bursa Malaysia Securities Berhad
By-Laws	:	By-laws governing the LTIP
CAGR	:	Compound annual growth rate, computed through the formula: CAGR = (Ending amount / Beginning amount)$^{1/N}$ – 1 Ending amount is the amount at the end of the period; Beginning amount is the amount at the beginning of the period; and N is the number of years within the period
CCM	:	Companies Commission of Malaysia
CDS	:	Central Depository System
China or PRC	:	The People's Republic of China, excluding for the purposes of this Prospectus only, the Hong Kong Special Administrative Region, the Macau Special Administrative Region of the People's Republic of China and Taiwan
CIMB IB	:	CIMB Investment Bank Berhad
CMSA	:	Capital Markets and Services Act 2007 of Malaysia
Constitution	:	Constitution of our Company
Conversion of ICPS	:	The conversion of 15,593,900 ICPS into 15,593,900 new Shares
Cornerstone Investors	:	Collectively, [●]
DG 12	:	Areca Dynamic Growth Fund 12
Depositor	:	A holder of a Securities Account
Directors	:	Directors of our Company and "**Director**" shall refer to any one of them
EBITDA	:	Earnings before interest, taxation, depreciation and amortisation
EDA Tools and Verification IP Suppliers	:	Collectively, Intelligent Circuit Engineering Sdn Bhd, Ansys, Inc and Siemens Electronic Design Automation Pte Ltd
Electronic Prospectus	:	Copy of this Prospectus that is issued, circulated or disseminated via the internet and/or an electronic storage medium including, but not limited to, CD-ROMs (Compact Disc - Read Only Memory)
Electronic Share Application	:	Application for our IPO Shares under the Retail Offering through a Participating Financial Institution's ATM
Eligible Persons	:	Collectively, our Directors, employees of our Group (including directors of our subsidiaries) and persons who have contributed to the success of our Group who are eligible to participate in the Retail Offering
Employee Share Sale and Purchase Plans or ESSPP	:	Share sale and purchase plans which allow the Key Employees to participate and become shareholders of our Company
EPS	:	Earnings per Share

DEFINITIONS *(Cont'd)*

Equity Guidelines	:	Equity Guidelines issued by the SC
ESG	:	Environmental, social and governance
ESIS	:	Employees' share issuance scheme for the issuance and allotment of ESIS Shares to the eligible Directors (excluding independent Directors) and eligible employees of our Group
ESIS Share(s)	:	New Share(s) to be allotted and issued to the Trustee that have been subscribed for by the Trustee pursuant to the ESIS
ESOS	:	Employees' share option scheme for the granting of ESOS Options to the eligible Directors (excluding independent Directors) and eligible employees of our Group
ESOS Option(s)	:	Right(s) to subscribe for our new Shares pursuant to the contract constituted by the acceptance of an offer made in accordance with the terms and conditions of the By-Laws
ESSPP SPV Shares	:	Ordinary shares in the respective ESSPP SPVs
ESSPP SPVs	:	Collectively, SKC Team, SKC Team 1, SKC Team 2 and SKC Team 3
Executive Director	:	Executive director of our Company
Final Retail Price	:	Final price per IPO Share to be paid by the Eligible Persons and investors under the Retail Offering, equivalent to the Retail Price or the Institutional Price, whichever is lower, to be determined on the Price Determination Date
Financial Years Under Review	:	Collectively, the FYEs 31 March 2023, 31 March 2024 and 31 March 2025
FYE	:	Financial year ended or where the context otherwise requires, financial year ending
Gobi	:	Collectively, Gobi Future Fund LPF, Meranti ASEAN Growth Fund II LP and Gobi Dana Impak Ventures LP
Government or Malaysian Government	:	Government of Malaysia
GB/s	:	Gigabyte per second
Gb/s	:	Gigabit per second
GP	:	Gross profit
IC Capital Management	:	IC Capital Management Sdn Bhd
IC Works	:	ICWorks Sdn Bhd
ICPS	:	Irredeemable convertible preference shares in our Company
IFRS	:	International Financial Reporting Standards issued by the International Accounting Standards Board

IMR Report	:	Independent market research report titled "Independent Assessment of the IC Design Industry" dated 17 October 2025 prepared by Vital Factor
IMR or Vital Factor	:	Vital Factor Consulting Sdn Bhd, the independent market and business research consultants
Initial Public Offering or IPO	:	Initial public offering comprising the Public Issue
Institutional Offering	:	Offering of 264,672,800 IPO Shares at the Institutional Price, subject to clawback and reallocation provisions, to institutional and selected investors
Institutional Price	:	Price per IPO Share to be paid by investors under the Institutional Offering which will be determined on the Price Determination Date by way of bookbuilding
Internet Participating Financial Institution(s)	:	Participating financial institution(s) for the Internet Share Application
Internet Share Application	:	Application for our IPO Shares under the Retail Offering through an Internet Participating Financial Institution or Participating Securities Firm
InterVest	:	Collectively, InterVest Global Scale-up Fund, Intervest Malaysia OIF A and Intervest Korea Malaysia OIF B Sdn Bhd
IPO Shares	:	New Shares to be issued by our Company under the Public Issue
Issuing House	:	Malaysian Issuing House Sdn Bhd
IT	:	Information technology
Joint Bookrunners	:	Collectively, CIMB IB and Maybank IB
Joint Underwriters	:	Collectively, CIMB IB and Maybank IB
Key Employees	:	Key employees who are vital to the future growth and performance of our Group
Key Senior Management	:	Key senior management of our Group, whose profiles are set out in Section 9.3.2 of this Prospectus and where applicable, Section 9.2.1 of this Prospectus
Keysight	:	Keysight Technologies Inc.
Keysight MY	:	Keysight Technologies Sales (Malaysia) Sdn Bhd
Keysight SG	:	Keysight Technologies Singapore (Sales) Pte Ltd
Lead Bookrunner	:	Maybank IB
Lion X	:	Lion X Investment VCC on behalf of Lion X Digital Innovation Investment Fund
Listing	:	Listing of and quotation for the entire enlarged issued Shares on the Main Market of Bursa Securities

DEFINITIONS *(Cont'd)*

Listing Requirements	:	Main Market Listing Requirements of Bursa Securities
LPD	:	19 September 2025, being the latest practicable date prior to the registration of this Prospectus with the SC
LTIP	:	Establishment of a long-term incentive plan of our Company comprising the ESOS and the ESIS which shall be administered in accordance with the By-Laws
Malaysia Digital Status	:	Malaysia Digital status granted by MDEC, a replacement of the former Multimedia Super Corridor status. Malaysia Digital Status companies are entitled to certain incentives, rights and privileges from the Government, subject to necessary approvals, compliance of applicable conditions, laws and regulations
Malaysian Public	:	Malaysian citizens, companies, co-operatives, societies and institutions incorporated or organised under the laws of Malaysia
Managing Underwriter	:	Maybank IB
Market Day	:	Any day on which Bursa Securities is open for trading in securities
Master Cornerstone Placement Agreement	:	Master cornerstone placement agreement between our Company, the Lead Bookrunner, the Joint Bookrunners and the Cornerstone Investors dated [●] as detailed in Section 4.2.2 of this Prospectus
Maybank IB	:	Maybank Investment Bank Berhad
MCCG	:	Malaysian Code on Corporate Governance issued by the SC
MDEC	:	Malaysia Digital Economy Corporation Sdn Bhd
MFRS	:	Malaysian Financial Reporting Standards issued by the Malaysian Accounting Standards Board
MIA	:	Malaysian Institute of Accountants
MITI	:	Ministry of Investment, Trade and Industry of Malaysia
MOF	:	Ministry of Finance Malaysia
Moratorium Providers	:	Collectively, Dato' Fong Swee Kiang, Teh Chee Hak, SKC Team, SKC Team 1, SKC Team 2, SKC Team 3 and the Voluntary Moratorium Shareholders, being shareholders of our Company whose securities will be held under moratorium
MPERS	:	Malaysian Private Entities Reporting Standard issued by the Malaysian Accounting Standards Board
MT/s	:	Mega transfer per second
N/A	:	Not applicable
nm	:	nanometre
Official List	:	A list specifying all securities listed on Bursa Securities
Participating Financial Institution(s)	:	A participating financial institution(s) for the Electronic Share Application

Participating Securities Firm(s)	:	A participating securities firm(s) for the Internet Share Application
PAT	:	Profit after taxation
PBT	:	Profit before taxation
PE Multiple	:	Price-to-earnings multiple
Pink Application Form	:	Application form for the application of our IPO Shares under the Retail Offering by the Eligible Persons accompanying this Prospectus
Pink Form Allocations	:	The allocation of 99,407,200 IPO Shares to the Eligible Persons under the Retail Offering
PIV Perkasa	:	PIV Perkasa Sdn Bhd
PIV Perkasa Allocation	:	Allocation of IPO Shares by our Company to PIV Perkasa, an entity nominated by SIDEC, amounting up to RM[●] million, representing approximately 0.4% of the enlarged issued Shares, at the Institutional Price
Placement Agreement	:	Placement agreement to be entered into between our Company, the Lead Bookrunner and the Joint Bookrunners in respect of such number of IPO Shares to be offered under the Institutional Offering
Price Determination Date	:	The date on which the Institutional Price and Final Retail Price will be determined
Principal Adviser	:	Maybank IB
Promoters	:	Collectively, Dato' Fong Swee Kiang and Teh Chee Hak and "**Promoter**" shall refer to any one of them
Prospectus	:	This Prospectus dated [●] issued by our Company
Prospectus Guidelines	:	Prospectus Guidelines issued by the SC
Public Issue	:	Public issue of 400,000,000 IPO Shares by our Company
R&D	:	Research and development
Record of Depositors	:	A record of securities holders established by Bursa Depository in accordance with the Rules of Bursa Depository
Retail Offering	:	Offering of 135,327,200 IPO Shares at the Retail Price, subject to the clawback and reallocation provisions, to be allocated in the following manner: (i) 99,407,200 IPO Shares reserved for application by the Eligible Persons; and (ii) 35,920,000 IPO Shares for application by the Malaysian Public, via balloting
Retail Price	:	Indicative initial price of RM[●] per IPO Share to be fully paid upon application under the Retail Offering, subject to adjustment as detailed in Section 4.3.1 of this Prospectus

Retail Underwriting Agreement	:	Retail underwriting agreement between our Company and the Joint Underwriters for the underwriting of the IPO Shares under the Retail Offering dated [●]
ROC	:	Registrar of Companies
Rules of Bursa Depository	:	The rules of Bursa Depository as issued under the SICDA
SAC	:	Shariah Advisory Council of the SC
SC	:	Securities Commission Malaysia
Securities Account or CDS Account	:	An account established by Bursa Depository for a Depositor for the recording of deposit of securities and for dealing in such securities by the Depositor
Share Registrar	:	Boardroom Share Registrars Sdn Bhd
SICDA	:	Securities Industry (Central Depositories) Act 1991 of Malaysia
SIDEC	:	SIDEC Sdn Bhd
SKC Team	:	SKC Team Sdn Bhd
SKC Team 1	:	SKC Team 1 Sdn Bhd (*formerly known as Euroxpress Sdn Bhd)*
SKC Team 2	:	SKC Team 2 Sdn Bhd (*formerly known as Odyssey Vision Sdn Bhd)*
SKC Team 3	:	SKC Team 3 Sdn Bhd
SkyeChip or Company	:	SkyeChip Berhad
SkyeChip Group or Group	:	Collectively, our Company and our subsidiaries
SkyeChip Shares or Shares	:	Ordinary shares in our Company
SOCSO	:	Social Security Organisation of Malaysia, also known as PERKESO (Pertubuhan Keselamatan Social)
sq ft	:	Square feet
Subdivision	:	Subdivision of 319,679,051 Shares into 1,396,000,000 Shares
TB/s	:	Terabyte per second
USA	:	United States of America
Voluntary Moratorium Shareholders	:	Collectively, Areca, InterVest, Gobi and Lion X

Currencies

RM and sen	:	Ringgit Malaysia and sen, the lawful currency of Malaysia
RMB	:	Renminbi, the lawful currency of the PRC
SGD	:	Singapore Dollar, the lawful currency of Singapore

USD	:	United States Dollar, the lawful currency of the USA
VND	:	Vietnam Dong, the lawful currency of Vietnam
Subsidiaries		
SkyeChip China	:	SkyeChip Semiconductor (Shanghai) Co., Ltd. (赛凯智半导体（上海）有限公司)
SkyeChip Singapore	:	SkyeChip Pte. Ltd.
SkyeChip Technology	:	SkyeChip Technology Sdn Bhd
SkyeChip Semi	:	SkyeChip Semi Sdn Bhd
SkyeChip Da Nang	:	SkyeChip Solutions Vietnam Company Limited
SkyeChip HCMC	:	SkyeChip Technology Vietnam Company Limited

GLOSSARY OF TECHNICAL TERMS

The following technical terms shall apply throughout this Prospectus unless the term is defined otherwise or the context requires otherwise:

Accelerator	:	A specialised hardware or IC designed to speed up a specific type of processing or task.
Advanced driver assistance systems (ADAS)	:	It is a technological system designed to enhance driving safety and to make driving simpler.
Algorithm	:	A step-by-step set of instructions or procedures to perform a task to achieve a desired outcome or to solve a problem.
Application-specific integrated circuits (ASIC)	:	It is a type of chip designed to run a specific task or application, as opposed to a general-purpose chip like a central processing unit. An ASIC is designed and optimised for a specific task or application, enabling enhanced performance, such as faster processing speeds and lower power consumption.
Artificial intelligence (AI)	:	It refers to systems or technologies that mimic human intelligence to perform tasks such as learning, reasoning and problem-solving. It encompasses techniques like machine learning and deep learning, which enable machines to analyse data, recognise patterns, and make decisions. AI systems may also incorporate inference engines, expert systems, and other advanced tools to simulate cognitive functions traditionally associated with human intelligence.
Bandwidth	:	In IC design, it is a measure of the speed of transfer of data in a given period, commonly in one second, between two devices or components within a chip.
Bit	:	A bit is short for binary digit and represents the most basic unit of data in digital computing. It can represent one of two possible values: either '1' or '0', or one of two states such as 'on' or 'off'.
Block	:	In the context of IC design, it refers to a distinct functional unit within the overall chip or circuit. Each block is designed to perform a specific task and communicates with other blocks to contribute to the overall operation of the IC.
Buffering	:	It is a technique used in computing systems to manage and optimise data flow between different components or processes. It involves temporarily storing data in memory areas known as buffers. This temporary storage helps manage data transfer between components that operate at different speeds or processing rates to smoothen data flow and prevent data loss or corruption.
Bus	:	In the context of IC design, a bus refers to a communication system that transfers data between various components within an IC or between different ICs. It uses a shared pathway to connect multiple components, enabling them to exchange data by sending and receiving signals.
Byte	:	A byte is a fundamental unit of digital information consisting of 8 bits. Each byte can represent various types of data, including characters, numbers, or symbols. For example, the character 'a' is represented in binary as 01100001. This 8-bit binary sequence constitutes one byte.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Central processing unit (CPU)	:	It is the primary processor in a computer or digital device, responsible for executing most of the processing tasks. It reads (retrieves) input data, processes it according to a set of instructions, and outputs the processed information to other components or devices, such as memory or display monitors.
Channel	:	In the context of IC design, it refers to a pathway within the IC to facilitate the movement or transfer of signals, data, or electrical current.
Channel configuration	:	In the context of IC design, it refers to the arrangement and setup of data transfer pathways within an IC. This configuration defines how different channels are structured, interconnected, and managed to facilitate efficient data exchange or signal transmission.
Chip	:	In the context of electronics, it refers to a small piece of semiconductor material, usually silicon that are also known as ICs. These ICs are made up of numerous electronically connected components such as transistors, resistors, diodes and capacitors that work together to perform various electronic functions.
Chiplet	:	It is a small, modular semiconductor component designed to perform a specific function within a larger IC or system on a chip. By combining multiple chiplets, designers can create flexible, scalable, and cost-effective solutions that leverage the strengths of different technologies.
Coherence	:	It refers to data consistency across multiple processors or cores accessing shared data.
Coherent Network-on-Chip	:	It is a network architecture within ICs that enables efficient data exchange between multiple cores or functional units while ensuring data consistency across all components. This coherence allows synchronised and reliable operation, which is critical for high-performance computing systems.
Compute-in-Memory silicon die (CIM silicon die)	:	It refers to a silicon product that perform computational operations directly within the memory arrays on the silicon die, integrating both data storage and processing functions in a single architecture.
Connection	:	In the context of ICs, connections are conductive paths that allow electrical signals to move between different components and devices on the chip. They enable communication and interaction between various parts of the circuit.
Core	:	In IC design, a core refers to a fundamental processing unit or functional block within a chip that carries out the specified operations or tasks assigned to it, as defined by its design and intended purpose.
Data packet	:	It is a small unit of data consisting of a header, content, and sometimes a trailer configured to be transmitted over a network. It facilitates the efficient and reliable transfer of data by dividing large messages into smaller chunks, to facilitate routing through one or several pathways, and reassembly at the destination.
Data path	:	In the context of an IC, it refers to the internal routes and components used to transfer, process, and manipulate data within the IC.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Data queue	:	A data queue is a data structure based on first-in-first-out used to manage and organise data or tasks sequentially. It ensures that data is processed in the order it was received and facilitates buffering and scheduling.
Data rate	:	It refers to the amount of data transmitted, processed or received over a communications link in a given period. The unit of measure is commonly bits/kilobits/megabits/gigabits per second or bytes/kilobytes/megabytes /gigabytes per second.
Debugging	:	A process for identifying, isolating and fixing any errors in a software, IC, hardware or system.
Die	:	In semiconductor chip fabrication, it is a small, individual piece of silicon that contains a complete IC. Multiple of the same ICs (dies) are etched onto a silicon wafer where each IC will constitute one die. After processing, each of the dies is cut out individually and each die, after packaging, will represent a separate chip in electronic devices.
Die-to-die (D2D)	:	In IC design, it refers to the connection for communication between different dies within a system. This is common in systems where multiple dies are needed to achieve the desired performance or functionality.
Digital signal processing (DSP)	:	It refers to the manipulation and analysis of digital signals using algorithms and mathematical operations. It involves converting analogue signals into digital form, processing these digital signals to extract useful information or improve quality, and then, if needed, converting them back into analogue form. DSP is widely used in various fields, including, among others, telecommunications, audio processing and image processing.
Double data rate (DDR)	:	It refers to a memory transfer technique that effectively doubles the data transfer rate compared to the traditional single data rate transfer method. DDR memory is commonly used in various electronic devices that require high memory bandwidth including personal computers, servers and network equipment. Different generations of DDR such as DDR3, DDR4, DDR4/5 and DDR5, offer different levels of performance, power efficiency and speed.
Dynamic random-access memory (DRAM)	:	It is a type of volatile memory that requires constant refreshing to retain data, making it suitable for memory in devices like computers and servers. It is valued for its high density, cost-effectiveness and random-access capability, making it a popular choice for system memory in a variety of digital devices such as desktops, laptops and servers, due to its ability to provide large amounts of memory at relatively low cost.
Electronic Design Automation (EDA) tools	:	It refers to software applications used to design ICs. These tools automate various aspects of the design functions.
Error correction code	:	It refers to a method of encoding data by adding redundant information, allowing the data to be recovered when it becomes corrupted during transmission or storage.
Fabrication	:	In the context of ICs, it is the process of manufacturing dies which are semiconductor chips that have not been packaged yet. The fabrication process involves the creation of the ICs onto a wafer commonly made of silicon, to form the final ICs which will be used in electronic devices.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Field-programmable gate array (FPGA)	:	It is a type of semiconductor chip designed to be programmed or reconfigured by the user after it has been manufactured. This capability provides the flexibility to tailor the chip for specific applications. Due to its adaptability, FPGAs are widely used for prototyping and for customising the functionality of electronic systems. An FPGA typically includes an array of programmable logic blocks, interconnects and I/O pins.
Foundry	:	It is a semiconductor manufacturing facility that produces ICs or chips and other semiconductor devices based on designs provided by other companies. Also referred to as a semiconductor foundry.
General-purpose input/output (GPIO)	:	It refers to pins on a computer board that can be configured by software to act as either an input or an output, allowing interaction with external circuits and devices.
Graphics processing unit (GPU)	:	It is a processor optimised for rendering graphics and performing parallel computations, widely used in gaming, AI and data analysis. Unlike the central processing unit (CPU), which is optimised for general-purpose tasks and sequential processing, the GPU is optimised for parallel processing and the execution of multiple tasks simultaneously, making it highly efficient for rendering graphics and performing calculations related to visual data. GPUs are now widely used in artificial intelligence due to their exceptional ability to handle complex computations efficiently. They are particularly instrumental in applications involving machine learning, deep learning, natural language processing, generative models, big data analytics and autonomous systems.
High-bandwidth memory (HBM) stacks	:	It refers to a collection of technologies or components designed to handle and facilitate the efficient transfer of large amounts of data at high speeds. This term is often used in the context of computer systems, networking and data processing where high data throughput is essential. HBM uses vertically stacked memory dies connected through silicon vias to achieve high data transfer rates and reduced power consumption. Among others, they are used in networking to achieve high data transfer rates, high-speed storage interface between storage devices and the central processing unit, and high-performance computing including parallel processing, video streaming, and virtual and augmented reality. Different generations of HBM such as HBM3, HBM3E and HBM4 offer different levels of performance and power efficiency.
Integrated circuit (IC)	:	It is commonly referred to as a chip or microchip and is a miniature electronic device consisting of interconnected transistors, resistors, capacitors and other components etched onto a tiny piece of semiconductor material, primarily silicon. These highly miniaturised circuits are designed to perform specific functions, ranging from data processing to controlling various electronic systems.
Input/Output (I/O)	:	In the context of IC design, it refers to the interfaces and mechanisms that allow an IC to communicate with external systems, devices, or other circuits.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Intellectual property (IP)	:	It refers to the original concepts, designs and technologies that are protected by legal rights such as patents, copyrights and trade secrets. This protection allows the designer to control the use, distribution and commercialisation of their innovative designs and technologies.
Interconnect	:	In the context of IC design, it refers to the connections used to link different components or functional blocks within a semiconductor device.
Interface	:	In the context of IC design, it refers to a method of communication and interaction between components, systems, subsystems or devices. This is to ensure that they all work together effectively.
Internet-of-things (IoT)	:	It refers to a network of interconnected physical devices that collect, exchange and process data over the internet without requiring direct human intervention. These devices, often embedded with sensors, software and communication technologies, can include anything from smart home appliances and wearable fitness trackers to industrial machines and autonomous vehicles.
Joint Electron Device Engineering Council (JEDEC) standards for memory	:	JEDEC standards define specifications for memory and other electronic components to ensure compatibility, performance and reliability. Notable JEDEC memory standards include those for DDR SDRAM (such as DDR3, DDR4, DDR4/5 and DDR5), HBM DRAM (such as HBM2, HBM3 and HBM4), LPDDR (such as LPDDR4, LPDDR4x, LPDDR5, LPDDR5x and LPDDR6) and other memory types used in storage devices. JEDEC memory standards address several key areas: - Physical characteristics: These standards define the dimensions and layout of memory modules to ensure compatibility with motherboards and other devices. They specify the function of each pin on the memory module, facilitating proper connection and communication with the system. - Electrical characteristics: JEDEC standards outline voltage levels, current requirements, signal timing, termination characteristics, and power management features. These specifications ensure that memory operates reliably and efficiently within the electrical constraints of the system. - Testing procedures: JEDEC standards include detailed testing protocols to verify that memory modules meet performance and reliability criteria. This encompasses tests for data integrity, timing margins, and environmental tolerance to ensure the memory performs as expected under various conditions.
Latency	:	It refers to the time delay between the initiation of a process and the completion of that process. It measures how long it takes for an operation to produce a result after a command or request has been issued. Latency is a critical performance metric in many aspects of IC design, particularly in memory, communication, and processing systems.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Low-power double data rate (LPDDR)	:	It refers to a series of memory standards designed to deliver high performance while consuming minimal power. These standards are primarily used in mobile devices, such as smartphones, tablets, and laptops, where power efficiency is crucial due to battery limitations. LPDDR memory achieves lower power consumption compared to traditional DDR memory by incorporating various power-saving features. Different generations of LPDDR such as LPDDR4, LPDDR4x, LPDDR5, LPDDR5x and LPDDR6 offer different levels of performance and power efficiency.
Low-voltage differential signalling (LVDS)	:	It refers to a data transmission standard that uses low voltage swings and differential signalling to transmit data efficiently, ensuring low power consumption and enhanced noise immunity.
Machine learning (ML)	:	It is a method where computers use specialised software and hardware to learn from large amounts of data. This learning process enables them to make decisions, analyse information, and provide answers to questions. It involves training algorithms to recognise patterns and improve their performance through repeated iterations and experience.
Memory controller	:	In the context of IC design for memory interfaces, a memory controller is a circuit that manages the communication between the computer's processor and its memory. It handles tasks like reading from and writing to memory, coordinating memory access, and ensuring that data is correctly stored and retrieved.
Memory interface	:	It refers to the set of protocols, electrical connections, and control mechanisms that facilitate communication between a processor (or other digital components) and memory modules. It defines how data is transferred to and from the memory, ensuring compatibility and proper functioning of the memory subsystem within a computer or electronic system.
Mobile Industry Processor Interface (MIPI)	:	It is a set of industry standards for interfaces in mobile devices to ensure efficient communication between components such as processors, cameras, and displays.
Module	:	It is a self-contained unit or component that performs a specific function and can be integrated into a larger system. Modules are designed to simplify design, facilitate modularity, and enhance system flexibility by allowing components to be added, removed, or replaced without affecting the overall system.
Network-on-Chip	:	It is a network system used in ICs particularly in SoC designs, to manage and optimise data transfer between different components or cores such as multiple processing units, memory blocks, and other functional modules within a single chip.
Neural network	:	It is a type of computer system that mimics the way the human brain works, consisting of layers of interconnected nodes (or "neurons") that process and learn from data. Neural networks are used for tasks like recognising images, understanding speech and making predictions by finding patterns in the data they are trained on.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Node	:	In the context of IC design, it refers to a technology node referring to the smallest structure or semiconductor component, such as a transistor that can be reliably produced on a silicon wafer. Technology nodes are a way to describe the size of the smallest structures that can be built using a particular manufacturing process. An example of a technology node would be a 7-nanometre (nm) or 5-nm node.
Non-coherent Network-on-Chip	:	It is a network architecture within ICs designed to manage communication between multiple cores or functional units but does not maintain data coherence or consistency across all the multiple cores or functional units.
Package	:	In the context of semiconductors and chips, packages are the protective enclosures that contain the die or ICs. They provide physical protection, electrical connections and help in heat dissipation.
PCI-SIG	:	Peripheral Component Interconnect Special Interest Group is an industry organisation responsible for specifying, standardising and promoting the Peripheral Component Interconnect (PCI), PCI-X, PCI Express (PCIe) and related interconnect technologies used in computing devices.
Physical layer (PHY)	:	It is a critical component of a communication system. It handles the physical connection to the communication medium such as electrical signals, optical signals or radio waves which represent data. It then will convert the data from digital form to analogue form or vice versa. It is also responsible for the transmission and reception of data and may include encoding, decoding, modulation and demodulation.
Power consumption	:	In the context of IC design, it refers to the amount of electrical power that an IC uses during its operation.
Power management	:	It refers to the techniques used to efficiently manage and optimise the power consumption of an IC. Effective power management is crucial for ensuring that an IC operates reliably, efficiently and within its thermal and power constraints.
Process design kit (PDK)	:	It is a comprehensive set of files, tools and documentation provided by a semiconductor foundry or technology provider. It describes the specific process technology used to fabricate ICs and serves as a crucial link between the IC design and manufacturing phases. The PDK enables IC designers to create layouts and circuits that are fully compatible with the fabrication process of the foundry. Each foundry provides its unique PDK tailored to its specific fabrication process, which means that IC designers must use the PDK associated with the particular foundry where their ICs will be manufactured.
Process nodes	:	It refers to semiconductor manufacturing technology and is commonly associated with the minimum distance between the centres of adjacent features on a chip, such as transistors and wiring connections. This measurement includes the size of the components and the spacing between them. It provides an indication of how dense and compact the chip can be made with the technology.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Protocol	:	A set of standardised rules and conventions that govern how data is transmitted, received and processed between devices or systems. Protocols ensure that communication between different entities is consistent, reliable and understandable, regardless of their underlying technology or design.
Random-access memory (RAM)	:	It is a type of computer memory that is used to store data or instructions that are actively being used or processed by processors. It is characterised by its ability to provide quick read (retrieve) and write (save) access to any location in the memory. It is also a volatile memory meaning it does not retain data without power, which differentiates it from non-volatile storage solutions used for long-term data retention. Unlike sequential access memory (such as magnetic tape), RAM allows data to be read or written in any order, without having to read through other data first.
Read	:	In the context of computing and digital systems, it refers to the retrieval of data.
Router	:	In the context of IC design relating to Network-on-Chip, it is a specialised component to manage and direct the flow of data packets across the various nodes within the chip. It is involved in managing data traffic ensuring that data is sent to the correct destination to facilitate communication. It is also involved in switching data packets across interconnected components of the chip.
RISC-V system-on-chip (RISC-V SoC)	:	It refers to a type of silicon product that incorporates RISC-V processor cores integrated with various silicon IPs. RISC-V is an open-standard Instruction Set Architecture (ISA) that defines how a processor works at the instruction level such as how it loads data or control program flow.
Signals	:	In the context of IC design, it refers to electrical currents or voltages that represent information and are transferred between different parts of the electric circuit. Signals can represent various types of information such as actual data, control, clock, power and address signals.
Silicon	:	It refers to the primary semiconductor material used in the fabrication of ICs and other electronic components. Silicon is a chemical element with the symbol Si and atomic number 14, and it is abundant in nature, and commonly found in sand and quartz.
Silicon intellectual property (Silicon IP)	:	It refers to pre-designed building blocks or modules that can be integrated into larger IC designs. These building blocks are pre-verified and reusable, helping to accelerate development and reduce design risks by providing tested and reliable building blocks. They vary from fundamental building blocks, such as arithmetic units and memory controllers, to more complex subsystems like communication interfaces.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Silicon products	:	In the context of IC design, it refers to final, functional ICs fabricated on silicon wafers, such as ASICs, CPUs, memory chips and other electronic components. These ICs may be stacked in the following configurations: - 2-dimension (2D), where the chips are placed side-by-side on a single plane. - 2.5-dimension (2.5D), where the chips are placed side-by-side on a silicon interposer that provides high-bandwidth interconnections between the chips. - 3-dimension (3D), where the chips are vertically stacked using through-silicon vias.
Stack	:	In the context of IC design, it refers to the three-dimensional (3D) stacking of multiple layers of IC to create a single compact and high-performance package. This technique also reduces latency and increases the density of electronic systems.
Static random-access memory (SRAM)	:	SRAM is a type of volatile memory (loses its data when power is turned off) that provides fast, reliable access to data without needing refresh cycles (required by dynamic random-access memory - DRAM), making it ideal for high-speed applications such as cache memory and embedded systems. However, its higher cost and larger size compared to DRAM limit its use in specific applications where performance is more critical than memory capacity.
Synchronous dynamic random-access memory (SDRAM)	:	SDRAM is a type of computer memory which offers faster data transfer rates compared to earlier versions of dynamic random-access memory (DRAM). SDRAM synchronises its operations with a system clock signal which allows for efficient data transfer and avoids potential timing issues. In the traditional approach in SDRAM, data is transferred only once per clock cycle (also known as single data rate), which limits the data transfer rate to the clock frequency. This has evolved to DDR SDRAM which can transfer data on both the rising and falling edges that enable doubling data rate within the same clock cycle. (For illustration it has 2 highway lanes for data traffic instead of one). JEDEC standards for SDRAM include DDR3, DDR4, DDR4/5 and DDR5. These standards specify features including data transfer rates, voltage requirements, timing parameters and common protocols.
System-on-chip (SoC)	:	It refers to an IC that integrates multiple components of an entire electronic system into a single chip. It combines multiple components and functions that are typically distributed across several chips into one compact, efficient package. Among others, it includes a CPU, GPU, memory and peripheral interfaces.
Tapeout	:	In IC design, it refers to the final step of the design process where the completed and finalised design is sent to the semiconductor foundry for fabrication.
Timing control	:	In the context of IC design, it refers to the mechanisms and techniques used to ensure that signals within the IC are synchronised and meet their required timing constraints. Proper timing control is crucial for the correct operation of digital circuits, as it affects how and when data is transferred and processed within the IC.

GLOSSARY OF TECHNICAL TERMS *(Cont'd)*

Universal Chiplet Interconnect Express (UCIe)	:	It is a set of industry standards that specifies a high-bandwidth interconnect for communication between heterogeneous chiplets within a single package.
Verification intellectual property (Verification IP)	:	It refers to pre-designed independent verification models to validate the compliance of silicon IP designs to industry standards and protocols such as JEDEC and UCIe. Verification IPs are used in conjunction with EDA tools.
Write	:	In the context of computing and digital systems, it refers to the saving of data.