7. BUSINESS OVERVIEW

7.1 HISTORY

The history of our business can be traced back to the establishment of SkyeChip in 2019, where we subsequently commenced IC design operations by developing silicon IPs in Penang in 2020.

The table below sets out the key events and milestones in the history and development of our business:

Calendar Year	Key Event and Milestone
2020	We commenced our IC design operations by developing silicon IPs. We secured our first contract for the design of memory interface IPs, namely DDR3 in 2020. We also secured our first contract for a custom silicon IP covering various interface protocols including DDR3 and DDR4 within a single IP. In the same year, we also initiated the design and development of memory interface IPs, namely HBM3. We initiated our first patent application for the invention of silicon IPs based on our design and development works. As at the LPD, we have developed a series of inventions, where 108 were filed for patent applications in Malaysia as well as in foreign countries including China and the USA. Out of these, 29 patents have been registered and 79 patents are pending application/registration.
2021-2022	In 2021, we initiated design and development works for the Network-on-Chip IPs. In 2022, we secured our first contract for coherent Network-on-Chip IP design and development, where we licensed our Network-on-Chip IP to a fabless semiconductor company. In 2022, we secured a contract for the design of a custom silicon IP covering various interface protocols including DDR, LPDDR, LVDS and MIPI.
2023-2024	In 2023, we secured a contract for the licensing of HBM3 memory interface IP, which includes a fully integrated controller, PHY and I/O. In the same year, we also secured a contract to develop a custom silicon IP, namely low-power low-latency memory interface IP. We also expanded into the design and development of custom ASIC. In 2023, we secured two contracts with a customer to jointly develop two IoT ASICs with the incorporation of our silicon IPs. In 2024, we expanded our silicon IP portfolio where we launched new and enhanced silicon IPs including HBM3E and a new generation of Network-on-Chip IP. In 2024, we secured a contract with a customer to develop custom ASIC for AI inference with the incorporation of our silicon IPs. In the same year, we commercialised our first IoT ASIC, which has completed the system and software development, pilot run and mass production. In 2024, we were granted the Malaysia Digital Status from MDEC for our IC design solutions. With the Malaysia Digital Status, we are entitled to certain incentives, rights and privileges from the Government of Malaysia, subject to necessary approvals, compliance of applicable conditions, laws and regulations.
2025	In January 2025, we joined the Intel Foundry Accelerator IP Alliance, which provides us with access to Intel Foundry's advanced process technologies, complementing our silicon IP design and development capabilities.

Calendar Year	Key Event and Milestone
	In July 2025, we expanded our silicon IP portfolio where we commercialised new silicon IPs, including D2D interface IP, as well as enhanced silicon IPs including LPDDR5 and LPDDR5x. In September 2025, we secured a contract for the development of RISC-V SoC, with the incorporation of RISC-V processor cores integrated with various silicon IPs, including our Network-on-Chip IP and other third-party silicon IPs.

7.2 AWARDS AND RECOGNITIONS

Since the commencement of our business in 2020 and up to the LPD, we have 29 patents registered in Malaysia, China and the USA, and 79 patents pending application/registration in Malaysia, China and the USA. See Annexure A of this Prospectus for further details on our patents.

Since the commencement of our business and up to the LPD, we have received the following awards and recognitions:

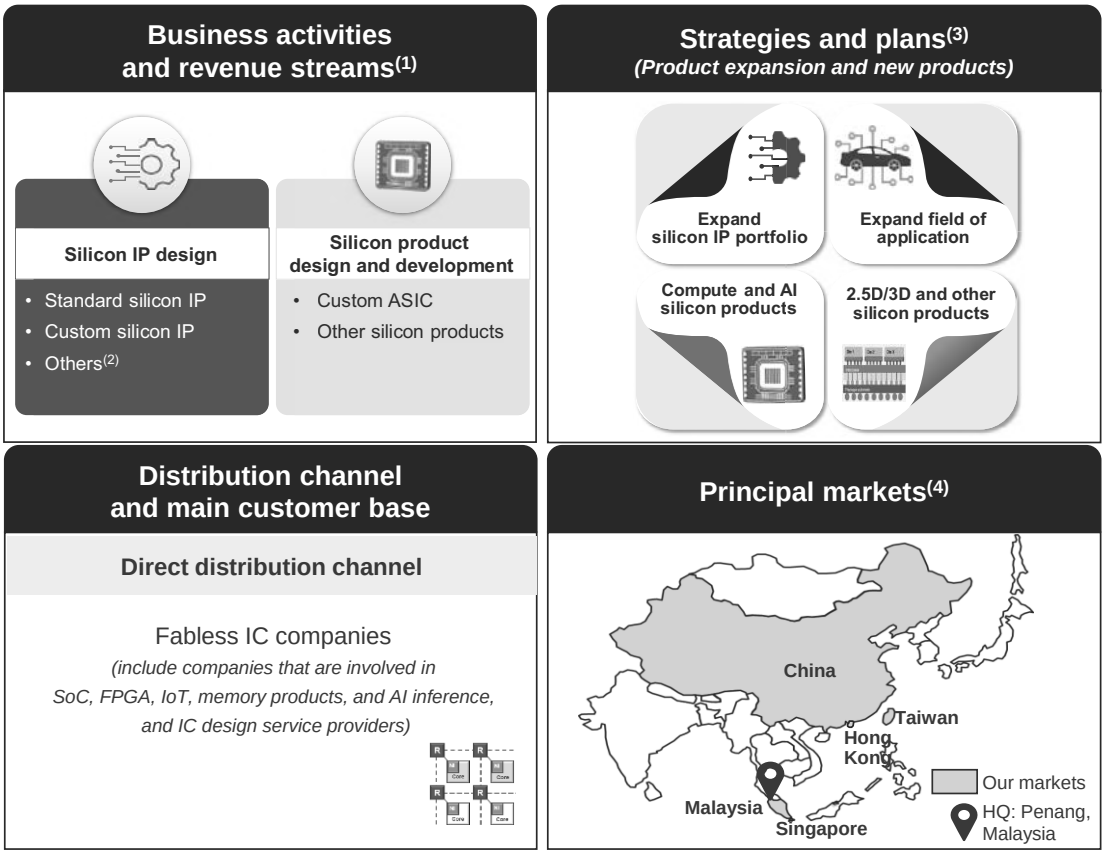
Year	Awarding party	Award / Recognition
2023	Ministry of Investment, Trade and Industry, Malaysia	Certificate of acknowledgement as a Mission-based Project Champion – Create global IC design champions in EV, RE and AI under the New Industrial Master Plan 2030
2023	The Institution of Engineering and Technology (Malaysia Network)	Platinum Award for Industry Excellence Award 2023

7. BUSINESS OVERVIEW *(Cont'd)*

7.3 OVERVIEW OF OUR BUSINESS

7.3.1 Our business model

Our business model is as follows:



Notes:

(1) *For the FYEs 31 March 2023 and 31 March 2024, our revenue was mainly contributed by the design of standard and custom silicon IPs. The design and development of custom ASIC commenced in September 2023. For the FYE 31 March 2025, the revenue contribution from the silicon IP design segment accounted for 73.3% of our total revenue, mainly from standard and custom silicon IPs, while the custom ASIC segment accounted for the remaining 26.7% of our total revenue.*

(2) *Include design services based on requests from customers for the FYEs 31 March 2024 and 31 March 2025, as well as design of memory test systems for the FYE 31 March 2025.*

(3) *See Section 7.5 of this Prospectus for details on our strategies and future plans.*

(4) *Revenue contribution from China accounted for 61.5%, 72.8%, and 56.5% of our total revenue for the FYEs 31 March 2023, 31 March 2024 and 31 March 2025 respectively. This is followed by Taiwan which accounted for 31.5%, 24.8%, and 33.5% of our total revenue for the FYEs 31 March 2023, 31 March 2024 and 31 March 2025 respectively. See Section 7.3.3 of this Prospectus for details of our revenue segmentation by geographical markets.*

7. BUSINESS OVERVIEW *(Cont'd)*

7.3.2 Business activities and revenue streams

We are principally involved in IC design specialising in silicon IPs and silicon products including custom ASIC. We provide licensable silicon IPs to our customers to integrate into their IC products. We also design and develop custom ASIC products tailored to meet specific customer requirements, delivering semiconductor chips that are optimised for a specific application rather than for general-purpose use.

As an original IC design company, we own the IP rights to our designs. As at the LPD, we have developed a series of inventions, of which 29 patents have been registered in Malaysia, China and the USA, and 79 patents are pending application/registration in Malaysia, China and the USA.

We have access to PDKs from foundries that enable us to design ICs on advanced process nodes down to 4nm. We also have access to interposer PDK and package design rules from OSAT partners, which allow us to carry out interposer and package design for 2.5D/3D packaging.

We use a range of IC design software tools and methodologies, including EDA tools to design, simulate, analyse and verify our IC designs. We also maintain and run our own server farms and computing infrastructure to support our IC design activities. As at the LPD, our IC Design and Software Design team consists of 318 technical personnel, including architects, logic design engineers, analogue circuit design engineers, physical design engineers, package design engineers and software engineers. Our team is led by our Chief Technology Officer, Teh Chee Hak.

Silicon IP refers to pre-designed and pre-verified building blocks or modules that can be integrated into larger IC designs. These building blocks are reusable and customisable, which help to accelerate development and reduce design risks of licensees by providing tested and reliable building blocks. Our designs adhere to international standard-setting bodies such as JEDEC and UCIe.

We are involved in IC design for standard and custom silicon IPs, where standard silicon IPs include memory interface IP, Network-on-Chip IP and D2D interface IP.

(i) Standard silicon IP

Our standard silicon IPs accounted for 44.6%, 62.4% and 62.6% of our total revenue for the FYEs 31 March 2023, 31 March 2024 and 31 March 2025 respectively. As our standard silicon IPs are to be integrated into our customers' IC products, our standard silicon IPs are designed in accordance with industry standards to ensure compatibility across various memory suppliers. These IP blocks are commonly used to accelerate the design process of larger ICs. Our standard silicon IP portfolio is as follows:

- **Memory interface IP:** Our memory interface IP manages data communications between the computing core and memory. When the computing core requires data, our memory interface IP retrieves it from the memory device and transfers it for processing. After processing, the memory interface IP sends the data back to the memory device for storage. Our memory interface IP includes a memory controller IP, a PHY IP and an I/O IP. This is a memory interface IP, which refers to self-contained blocks designed for efficient memory management.

- **Network-on-Chip IP:** We design Network-on-Chip interconnect IP that focus on both physical and logical infrastructure to ensure efficient data routing within a SoC. Network-on-Chip serves as the communication pathway connecting multiple components within a SoC. Our Network-on-Chip IPs are configurable to meet specific application needs and performance requirements. We provide IC design for both coherent and non-coherent Network-on-Chip IPs.

7. BUSINESS OVERVIEW *(Cont'd)*

- **D2D interface IP:** Our D2D interface IP is designed to facilitate high-speed communication between different functional blocks within a multi-die package, such as a CPU, GPU and FPGA, or other processors configured in 2D, 2.5D or 3D structures. Our D2D interface IP includes both a controller and PHY block.

To support the integration and configuration of our standard silicon IPs, we offer in-house proprietary memory system firmware solutions.

(ii) Custom silicon IP

Our custom silicon IPs accounted for 55.4%, 36.6% and 9.2% of our total revenue for the FYEs 31 March 2023, 31 March 2024 and 31 March 2025 respectively. Our custom silicon IPs are designed based on individual customer specifications and requirements, which will be integrated into our customers' IC products. This includes multi-interface protocol IPs that support different standards and communication protocols such as DDR, LPDDR, MIPI, LVDS and multi-standard I/O interfaces.

In addition, we have designed and developed a custom low-power, low-latency memory interface IP tailored for specific applications. This IP is optimised to minimise power consumption and enhance memory protocol handling, thereby improving data flow between computing cores and memory. To support the integration and configuration of our custom silicon IPs, we offer in-house proprietary memory system firmware solutions.

(iii) Silicon products

Custom ASIC

We expanded into the design and development of custom ASIC in September 2023. A custom ASIC is a semiconductor chip designed for a specific application rather than for general-purpose use. For the FYE 31 March 2025, revenue contribution from the custom ASIC segment accounted for 26.7% of our total revenue.

Custom ASIC is designed to perform targeted functions with enhanced efficiency in power consumption and performance, a reduced physical footprint and the ability to execute proprietary algorithms that standard devices are unable to support efficiently. Additionally, custom ASIC provides improved IP protection as functionality is embedded at the hardware level, safeguarding proprietary technology and processes from reverse engineering.

Other silicon products

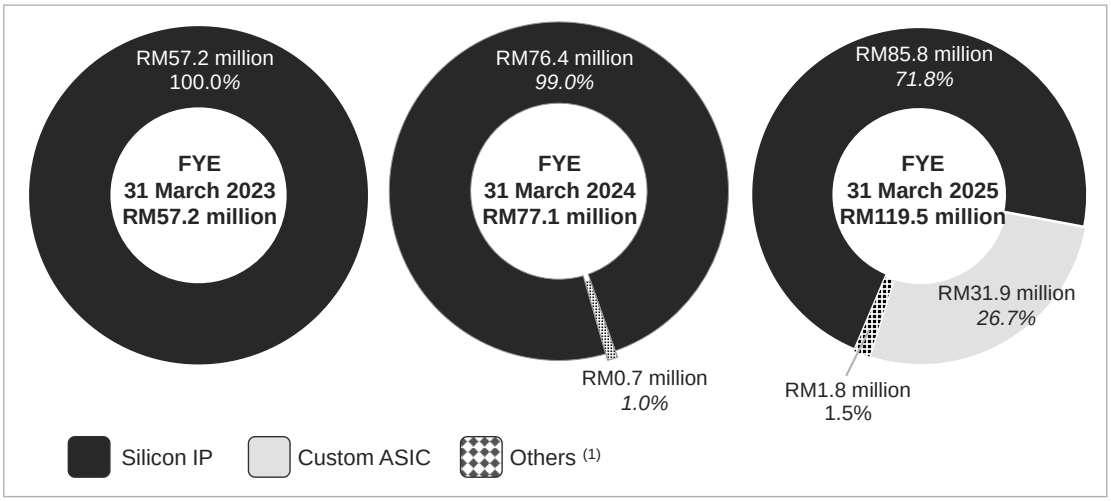
In September 2025, we expanded into the development of other silicon products, where we secured a contract for the development of RISC-V SoC. This development involves the incorporation of RISC-V processor cores integrated with various silicon IPs, including our Network-on-Chip IP and other third-party silicon IPs.

(iv) Others

Revenue from the others segment accounted for 1.0% and 1.5% of our total revenue for the FYEs 31 March 2024 and 31 March 2025 respectively. This includes design services based on requests from customers as part of our integrated customer support services, as well as design of memory test systems.

7. BUSINESS OVERVIEW *(Cont'd)*

For the Financial Years Under Review, our revenue segmentation by products and services is depicted below:



***Note**:*

(1) Include design services based on requests from customers for the FYEs 31 March 2024 and 31 March 2025, as well as design of memory test systems for the FYE 31 March 2025.

Further breakdown of our revenue segmentation by products and services is set out in the table below:

	FYE 31 March					
	2023		2024		2025	
Revenue	**RM'000**	%	**RM'000**	%	**RM'000**	%
Silicon IP segment	57,159	100.0	76,327	99.0	85,739	71.8
Standard silicon IP (1)	*25,486*	*44.6*	*48,115*	*62.4*	*74,771*	*62.6*
Custom silicon IP	*31,673*	*55.4*	*28,212*	*36.6*	*10,968*	*9.2*
Custom ASIC segment	-	-	-	-	31,934	26.7
Others	-	-	736	1.0	1,830	1.5
Total revenue	**57,159**	**100.0**	**77,063**	**100.0**	**119,503**	**100.0**

Note:

(1) Includes memory interface IP and Network-on-Chip IP, of which the breakdown for the Financial Years Under Review is as follows:

	FYE 31 March					
	2023		2024		2025	
Revenue	**RM'000**	%	**RM'000**	%	**RM'000**	%
Memory interface IP	7,482	13.1	28,099	36.4	47,169	39.5
Network-on-Chip IP	18,004	31.5	20,016	26.0	27,602	23.1
Total	**25,486**	**44.6**	**48,115**	**62.4**	**74,771**	**62.6**

7. BUSINESS OVERVIEW *(Cont'd)*

7.3.3 Principal markets

We principally operate in Penang, Malaysia and mainly serve foreign customers. Within foreign markets, China and Taiwan collectively accounted for 93.0%, 97.6%, and 90.0% of our total revenue for the FYEs 31 March 2023, 31 March 2024 and 31 March 2025 respectively. This is followed by Singapore at 2.4% and 1.0% of our total revenue for the FYEs 31 March 2024 and 31 March 2025 respectively, and Hong Kong at 0.9% of our total revenue for the FYE 31 March 2025. Meanwhile, Malaysia accounted for 7.0% and 8.1% of our total revenue for the FYEs 31 March 2023 and 31 March 2025 respectively.

The breakdown of our revenue by geographical markets for the Financial Years Under Review is as follows:

	FYE 31 March					
	2023		2024		2025	
	RM'000	%	RM'000	%	RM'000	%
Foreign markets	**53,175**	**93.0**	**77,063**	**100.0**	**109,799**	**91.9**
China	35,171	61.5	56,124	72.8	67,473	56.5
Taiwan	18,004	31.5	19,136	24.8	39,997	33.5
Singapore	-	-	1,803	2.4	1,237	1.0
Hong Kong	-	-	-	-	1,092	0.9
Malaysia	**3,984**	**7.0**	**-**	**-**	**9,704**	**8.1**
Total revenue	**57,159**	**100.0**	**77,063**	**100.0**	**119,503**	**100.0**

7.3.4 Distribution channels and customers

We utilise a direct distribution channel strategy, securing contracts directly with customers who use our products and services. Our customers are fabless IC companies including companies that are involved in SoC, FPGA, IoT, memory products and AI inference, as well as IC design service providers. Our direct distribution channel strategy enables us to work closely with customers to address their specific needs and specifications. Additionally, we provide customised solutions and services, including design support for integration and implementation. This approach fosters strong customer relationships and also positions us to secure more projects from each customer.

For the Financial Years Under Review, all our revenue was derived from direct distribution channels where our revenue by customer type is as follows:

	FYE 31 March					
	2023		2024		2025	
	RM'000	%	RM'000	%	RM'000	%
Direct distribution channel	**57,159**	**100.0**	**77,063**	**100.0**	**119,503**	**100.0**
Fabless IC companies	57,159	100.0	77,063	100.0	119,503	100.0
Total revenue	**57,159**	**100.0**	**77,063**	**100.0**	**119,503**	**100.0**

7.4 OUR COMPETITIVE STRENGTHS

Our competitive strengths which will provide us with the platform to sustain and grow our business, are as follows:

7.4.1 We have designed and commercialised multiple high-performance and high-bandwidth memory interface IP to drive our business growth and sustain our competitive advantages

As at the LPD, we have designed and commercialised multiple high-performance, high-bandwidth memory interface IPs, including LPDDR4, LPDDR4x, LPDDR5, LPDDR5x, as well as HBM3 and HBM3E. These memory interface IPs deliver efficient data transfer and meet the rigorous demands of advanced applications, which drive our business growth and strengthen our competitive position in the semiconductor industry.

In addition, we continue to develop the next generations of memory interface IPs, including LPDDR6 and HBM4. These advancements will facilitate the continuing relevance of our services to meet ever-increasing improvements in performance as well as to sustain and grow our business.

7.4.2 We have access to advanced technologies down to a 4nm process node supported by foundries as well as certain third-party design tool providers

As an IC design company, it is essential for us to stay at the forefront of technological changes, innovations and advancements, particularly in the fast-evolving field of ICs and electronics. The short product life cycles of electronic devices often drive the demand for greater processing power while reducing device size, requiring more components, such as transistors, to fit into smaller semiconductor areas.

We have access to PDKs from foundries to design ICs using advanced process nodes down to 4nm. These PDKs supply essential design rules, simulation models and documentation that ensure our designs meet manufacturability and yield requirements. In addition, we also have access to EDA tools and Verification IPs from third-party design tool providers. EDA tools and Verification IPs are specialised and essential tools for IC design. See Section 7.13 of this Prospectus for further details on the technologies used.

In addition to our IC design operation, access to advanced technologies is crucial for our new ventures into custom ASIC design and development, especially for applications requiring high performance, power efficiency and a smaller form factor. This capability is demonstrated by our successful tapeout of two IoT ASICs, which had incorporated our silicon IPs. As at the LPD, the prototypes of our IoT ASICs were completed in April 2024 and September 2024 respectively. One of these IoT ASICs has been commercialised in September 2024 and the second IoT ASIC is planned for commercialisation by end-2025.

Access to advanced technologies gives us a significant advantage by enabling us to meet the technological requirements of a diverse customer base, thus supporting our business growth. Additionally, these advanced technologies enhance our internal R&D efforts, allowing us to develop innovative IC designs that can address emerging business opportunities and sustain our growth.

7.4.3 We are the original designer of our standard silicon IP featuring reconfigurability which enables us to license our products to multiple customers, providing us with a modular and scalable business model to sustain and drive our business growth

We have designed and commercialised standard silicon IPs, including memory interface IP, Network-on-Chip IP and D2D interface IP, which were developed in-house entirely. As such, we retain full IP rights to these designs. Our library of standard silicon IPs allows for scalable business growth, as each silicon IP can be licensed as is or reconfigured to meet each customer's operating environment across various countries. This silicon IP enables us to license them to multiple customers or projects, providing a robust portfolio that supports and drives our business growth. This approach offers a significant business advantage, as it eliminates the need to invest substantial time and resources in developing each silicon IP for each new customer.

Our standard silicon IP is configurable, allowing us to customise it to meet each customer's specific needs while still conforming to industry standards. This flexibility ensures that our IP can be reused across a range of applications and customers with minimal modifications. We launched our standard silicon IP in 2022 (FYE 31 March 2023) and our revenue from standard silicon IP increased by 88.8% to RM48.1 million for the FYE 31 March 2024 (FYE 31 March 2023: RM25.5 million), followed by further growth of 55.4% to RM74.8 million for the FYE 31 March 2025.

Our current business model involves right-to-use sales of our silicon IP, while retaining the intellectual property rights to these designs. Customers are granted the right to use our IP exclusively for the specific projects outlined in their licensing contracts. This approach not only ensures ongoing ownership of our IP but also provides an opportunity for additional revenue if our IP is used in other products or projects.

7.4.4 We have successfully commercialised both coherent and non-coherent Network-on-Chip IPs which will help grow our business

Network-on-Chip IP is essential for managing on-die communication infrastructures in complex multi-core ICs, ensuring high-efficiency, high-performance and low-power data transactions. Our Network-on-Chip technology provides us with the platform to address increasingly complex IC designs as chips move towards more advanced process nodes carrying out more extensive processing requiring efficient and quality transmission and reception of data in SoC. This will provide relevance to our design in meeting changing and innovative technologies to grow our business.

Our Network-on-Chip technology offers several advantages over traditional interconnect methods such as bus-based, point-to-point, hierarchical, ring, and cross-bar switches. These advantages include improved scalability, performance, modularity, flexibility, fault tolerance and power efficiency. As a result, Network-on-Chip is a popular choice for modern SoC designs, especially in systems with high complexity and performance demands. See Section 7.7.6 of this Prospectus for more details on the benefits of Network-on-Chip.

In addition, we offer both coherent and non-coherent Network-on-Chip IPs, enabling us to support a wide range of IC products. We have the capability to integrate both coherent and non-coherent Network-on-Chip architectures within the same chip. This dual capability allows us to address a broader market, including high-performance computing, AI and consumer electronics. See Section 7.7.6 of this Prospectus for more details on the coherent and non-coherent Network-on-Chip IPs.

Our expertise in designing both coherent and non-coherent Network-on-Chip IPs is crucial for our business growth. This capability requires advanced skills and provides us with a significant competitive edge to meet the evolving market demands. Our capabilities are further enhanced by the commercialisation of our latest Network-on-Chip IPs in 2024. These latest Network-on-Chip IPs includes non-coherent Network-on-Chip IP with expanded protocol support and improvements in power, performance and area, as well as coherent Network-on-Chip IP with enhanced topology support to reduce latency.

Our coherent and non-coherent Network-on-Chip IPs are engineered for high bandwidth, low power consumption and reduced latency in multi-processor semiconductors. They offer flexible configuration and reliable performance, making them highly attractive to potential customers and driving our business growth. Additionally, we plan to leverage our non-coherent Network-on-Chip architecture to explore new applications in the automotive sector in the future.

7.4.5 We have in-house developed proprietary software that provides ease of use to configure our Network-on-Chip IP into our customers' ICs

We have our in-house developed proprietary software to support the configuration of our Network-on-Chip IP into our customers' ICs. Our proprietary software is typically packaged with our Network-on-Chip IP for use by our customers, which are tools designed to optimise system performance for configuration and integration. See Section 7.7.6 of this Prospectus for more information on our in-house developed proprietary software.

Our in-house developed proprietary software, bundled with our Network-on-Chip IP, offers convenience to our customers by simulating and optimising interconnect performance, as well as ensuring seamless integration of our Network-on-Chip IP into their overall ICs. This software, RAPTuner, is designed to add value to our Network-on-Chip IP, enhancing its appeal and encouraging the purchase of our Network-on-Chip IP.

7.4.6 We have experienced Executive Directors backed by a skilled technical team to sustain and further develop our business

Our business is led by our Chief Executive Officer, Dato' Fong Swee Kiang and Chief Technology Officer, Teh Chee Hak.

Dato' Fong Swee Kiang has over 35 years of experience in the semiconductor industry. He has held positions at the Intel group of companies where he was responsible for overseeing the development of central processing units, chipsets and IPs, while leading a team of engineers. Additionally, he has worked at Altera Corporation (M) Sdn Bhd ("**Altera Malaysia**"), an Intel Corporation related company following its acquisition of Altera Corporation in 2015, leading the company's R&D operations in Malaysia, driving innovation and development initiatives. He has also served as Director of Operations and Senior Operations Director at Avago Technologies (Malaysia) Sdn Bhd ("**Avago Technologies**"), a Broadcom Inc. related company, managing the company's global operations and overseeing new product introductions before founding SkyeChip which commenced business in 2020. He is responsible for leading our Group's business strategy, overseeing operations, sales and marketing and ensuring financial health while managing our Group's business and investment stakeholders.

Teh Chee Hak has over 20 years of experience in the semiconductor industry. He began his career at Intel Microelectronics (M) Sdn Bhd ("**Intel Microelectronics**"), where he was responsible for the architecture and microarchitecture of central processing units, memory, I/O and platform controller hubs and IPs, as well as completing assignments in the USA. He then joined Altera Malaysia as a principal engineer before progressing to the role of architect where he was responsible for designing and implementing the memory interface architecture and microarchitecture of FPGA products and IPs. He transitioned back to Intel Microelectronics as a principal engineer and subsequently served as chief architect at Intel Microelectronics where he focused primarily on the overall architecture and microarchitecture of FPGA products and IPs. He joined SkyeChip in 2020 where he is responsible for overseeing our Group's technical strategy and leading the design and development of advanced IPs and ASICs for AI and high-performance computing applications.

As at the LPD, our technical team comprises 318 professionals who hold degrees, diplomas or certificates in relevant disciplines. Our team is led by our Chief Technology Officer, Teh Chee Hak. These technical experts are essential in our design and development operations, as well as providing engineering support to our customers.

See Section 9 of this Prospectus for further details on our Executive Directors and technical personnel.

7.4.7 Our business has experienced high revenue growth demonstrating the acceptance of our products and services to serve as the platform for further business growth

Since the commencement of our business in 2020, we have shown consistent revenue growth. From the FYEs 31 March 2023 to 31 March 2025, our revenue increased at a CAGR of 44.6%, reaching RM119.5 million for the FYE 31 March 2025. This robust revenue growth reflects the strong market acceptance of our products and services and provides a solid platform for further expansion. Building on the success of our current suite of silicon IPs, we are actively developing several new products to drive continued growth. See Section 7.5 of this Prospectus for further details of our strategies and future plans.

We continue to capitalise on our competency in silicon IP design by investing in innovation and integrating our silicon IPs with new product developments. This approach not only enhances our silicon IP offerings but also allows us to expand into ASIC design and development. By demonstrating our adaptability and technical expertise, we are able to drive growth and explore new opportunities in the industry. This is demonstrated by our contracts secured with customers for the design and development of two IoT ASICs and an AI inference ASIC. These contracts bundle our silicon IP with our ASIC design capabilities, demonstrating our ability to integrate both hardware and IP effectively. See Sections 7.7.8 to 7.7.10 of this Prospectus for further details.

Our expertise in silicon IP design includes supporting and ensuring interoperability for multiple interface protocols and specific interface requirements, while optimising power, performance and area for various applications. Additionally, our ability to design and validate IP in accordance with industry standards such as JEDEC and UCIe enhances our reputation for technical competence. This serves as a platform to secure new contracts, driving business growth and expanding our revenue base in the future.

7.4.8 We have the ability to provide custom silicon IP for our customers to foster customer loyalty and secure new contracts

One of our key strengths is our technical expertise in designing custom silicon IP tailored to meet the specific requirements of each customer. This includes optimising performance, power efficiency and functionality needs, as well as the ability to modify and enhance designs based on customer feedback and evolving requirements. We provide comprehensive support including design, integration and prototype bring-up assistance to facilitate the productisation of our customers' IC products. This capability fosters customer loyalty and helps us secure new business opportunities.

Our strengths are supported by our team of technical personnel with expertise and knowledge in various aspects of silicon IP design and IC development. Our technical personnel including engineers increased from 38 personnel in 2020 to 318 personnel as at the LPD.

Furthermore, our custom silicon IP offerings allow us to provide optimised solutions to customers of a wide range of electronic products ranging from consumer products, such as wearable devices, to industrial and communication applications, as well as IoT and AI applications. This will provide us with a potentially large addressable market to grow our business as well as to mitigate against risks of a downturn in one or a small number of user groups or sectors.

Revenue contribution from our custom silicon IP accounted for RM31.7 million (55.4%), RM28.2 million (36.6%) and RM11.0 million (9.2%) of our total revenue for the FYEs 31 March 2023, 31 March 2024 and 31 March 2025 respectively. Our ability to successfully deliver our custom silicon IP serves as a platform to grow our business and customer base.

7.4.9 We are engaged in various industry standard definition bodies including JEDEC, UCIe and PCI-SIG that enable us to participate in early discussions on the evolving IP standards

Industry standard bodies such as JEDEC, UCIe and PCI-SIG are essential for IP as they ensure interoperability and compatibility, which is crucial for integrating various IPs and modules into a functional system. Therefore, incorporating these standards into our IP design is vital to ensure interoperability and compatibility for market acceptance to support the sustainability and growth of our business.

As a member of JEDEC, UCIe and PCI-SIG, we are involved in defining and reviewing the emerging standards. Our involvement with these global standard-setting bodies provides us with advanced insights into emerging trends, potential revisions and new standards. This enables us to proactively adapt our designs to evolving requirements, ensuring that we remain competitive and relevant, and continue to grow our business.

7.5 OUR STRATEGIES AND FUTURE PLANS

In 2024, Malaysia's electrical and electronic (E&E) exports recorded RM601.6 billion, with electronic ICs accounting for 52.0% of the total E&E exports. Malaysia's semiconductor strength primarily lies in its back-end services, such as assembly, packing and testing. A key strategic development of the New Industrial Master Plan 2030 (NIMP 2030) is to elevate Malaysia's position within the E&E value chain by shifting towards front-end activities such as IC design, advanced packaging and expanding wafer fabrication capabilities. *(Source: IMR Report)*

Our strategies and future plans are aligned with the NIMP 2030 to enhance high-value-added activities within the semiconductor and electronics industry value chain. NIMP 2030 was launched in 2023 to strengthen IC design capabilities, enabling Malaysia to capitalise on rapidly growing sectors such as electric vehicles, renewable energy and AI *(Source: IMR Report)*.

Going forward, we will leverage our expertise in silicon IP and IC design to capitalise on both existing and new opportunities in the IC design and semiconductor industry. We will also stay relevant with technological innovations to drive our business expansion and growth.

Overview of our strategies and future plans

7.5.1 Expansion of silicon IP portfolio and field of application

(a) Expand silicon IP portfolio

Our strategies and future plans are to capitalise on our competency in standard and custom silicon IP by continuing to invest in silicon IP innovations. We plan to expand our silicon IP portfolio to drive business growth and increase our revenue base. This expansion includes designing and developing a new generation of Network-on-Chip IP and memory interface IP.

We have successfully designed and delivered multiple custom silicon IPs that incorporate multiple memory interface standards within a single IP. As at the LPD, we have successfully designed and commercialised multiple memory interface IPs, including LPDDR4, LPDDR4x, LPDDR5, LPDDR5x, as well as HBM3 and HBM3E. These represent some of the current versions of the memory interface IPs with high data throughput that supports advanced computing requirements. Our capabilities are further demonstrated by the commercialisation of our latest Network-on-Chip IP in 2024, which includes coherent and non-coherent Network-on-Chip IPs. This new generation Network-on-Chip IP feature expanded protocol support, improved power efficiency, enhanced performance, and reduced latency and area, making them ideal for a wide range of applications, from edge computing to data centres.

We carry out continuous R&D to keep abreast of evolving technologies to improve the performance of our memory interface IPs. As part of our strategies and future plans, we aim to develop new memory interface IPs, including LPDDR6 and HBM4, in the future, featuring improved efficiency and performance, and increasing data transfer rates. This will help us meet growing demand for end-market applications such as mobile and consumer electronics, networking, edge computing and high-performance computing.

7. BUSINESS OVERVIEW *(Cont'd)*

The table below depicts our strategies and future plans to develop new generations of memory interface IPs with the target specifications as below:

Target specification	Double Data Rate					High Bandwidth Memory		
	LPDDR4	LPDDR4x	LPDDR5	LPDDR5x	LPDDR6(1)	HBM3	HBM3E	HBM4(1)
Maximum data rate (Gb/s)	3.2	4.267	6.4	≥8.5	14.4	6.4	≥8.0	≥8.0
Total data width per component	64	64	64	64	96	1024	1024	2048
Maximum total bandwidth (GB/s)	25.6	34.1	51.2	≥68.3	172.8	819	≥1024	≥2048
Energy efficiency (pJ/bit)	~7-10	~7-10	~5-7	~2-3	~2-3	~0.6	~0.6	~0.4-0.5

Note:
(1) The target specification for intended products

Note: Values in the table are approximate and can vary based on specific implementation, operating condition and workload characteristics

We are leveraging our expertise in software and firmware development to venture into the EDA tool licensing model in the future to establish a new revenue stream. In addition to Network-on-Chip IP design and development, we provide technical assistance with the use of our in-house developed proprietary software to support the integration and configuration of our Network-on-Chip IP into our customers' ICs. Our proprietary software is typically packaged with our Network-on-Chip IP for use by our customers. Our in-house designed and developed integration and configuration software includes RAPTuner (a network architecture simulation and optimisation tool).

Our existing knowledge in silicon IP design is complemented by proprietary EDA tools that are designed specifically for optimisation, verification and validation. This will offer customers a complete silicon IP design suite that integrates IP configuration, testing and performance analysis. The development of EDA tools that are pre-integrated with our own silicon IP will streamline the process for our customers who use our silicon IP in their design.

(b) Expand new field of application – automotive silicon IP

Our current silicon IP portfolio is designed to meet the needs of high-performance computing, mobile communications, IoT, AI and data centre applications. As part of our strategic expansion, we plan to expand into the automotive IP market to capitalise on the growing opportunities, driven by the increasing demand for advanced automotive technologies.

The new automotive IP will be able to support critical technologies such as in-vehicle networks and vision systems, which are essential for ADAS and autonomous driving. These technologies enable accurate and comprehensive information transmission within vehicles, ensuring safety, power efficiency and performance.

A key focus of the automotive IP development will be on our Network-on-Chip IP. To meet the requirements of the automotive industry, the new silicon IP is required to adhere to functional safety standards, including compliance with ISO 26262. As at the LPD, our team is in the process of refining the IP to meet the requirements and we plan to commercialise the new automotive silicon IP between 2026 and 2027.

The estimated cost for our silicon IP portfolio expansion and new field of application expansion is approximately RM[●] million for a period of 36 months from the date of our Listing between 2026 and 2029, which will be funded through the gross proceeds from our Public Issue. See Section 4.5 of this Prospectus for further details on the use of proceeds.

7. BUSINESS OVERVIEW *(Cont'd)*

7.5.2 Design and develop compute and AI silicon products

We plan to design and develop new compute and AI silicon products to address the rising demand for high-performance, energy-efficient processing in data centres and AI applications. This is done by incorporating our pre-designed and pre-verified interface and interconnect silicon IP which will lead to faster development times compared to developing everything from scratch.

The new compute and AI silicon products will focus on two segments as described below:

(i) Custom compute and AI hardware accelerator

Custom compute and AI hardware accelerators are ASICs designed for AI and large-scale data workloads. They offload specialised tasks, such as tensor math and input data preprocessing, from general-purpose CPUs/GPUs into dedicated hardware engines. This approach offers the flexibility needed to handle large-scale data operations while improving overall system efficiency and reducing overall power consumption. Key examples include:

- Data preprocessing hardware accelerator: A dedicated hardware that processes raw data before it reaches the AI or compute engine. It handles data formatting, cleaning, resizing, compression, and error checking, which reduces data transfer and power consumption while enabling the main processors to focus on computational workloads.

- Security ASIC products: Custom-designed products optimised for cryptographic operations, secure processing and hardware-based security functions. These ASICs are widely used in trusted computing, secure communications, authentication and anti-tampering applications.

The development process involves integrating our interface and interconnect IPs with third-party IPs, and customers' proprietary IPs. To expand our custom ASIC offerings, we plan to enter into joint-development arrangements with technology partners. These partnerships will allow us to tap into their system architecture and software expertise, complementing our silicon IP design and development capabilities. As at the LPD, we have not entered into any arrangements for the joint development of new compute and AI hardware accelerators.

(ii) High-performance CPU and AI platforms

We also plan to expand our silicon products to develop high-performance CPU and AI platforms that combine CPU-grade general computing capabilities and AI acceleration for the server and edge computing environment.

In March 2025, Malaysia announced a 10-year partnership worth USD250 million (approximately RM1.1 billion) with ARM Holdings Plc ("**ARM**") to acquire various IP licences, including 7 ARM Compute Subsystem ("**CSS**") and 25 ARM Flexible Access ("**AFA**") tokens, and to train 10,000 engineers. This is part of the national initiative, Silicon Vision, which offers opportunities for semiconductor and IC design companies to participate and grow within the local ecosystem. As at the LPD, we have submitted our application for access to one CSS platform and one AFA platform, and is currently pending the decision of relevant regulatory authorities.

In line with our strategy to expand our silicon product offerings, we plan to design and develop new high-performance CPU and AI platforms. High-performance CPU and AI platforms are designed to optimise performance for a server and edge computing environment.

By leveraging our technical expertise and strength in memory interface and Network-on-Chip IPs, the development of the new high-performance CPU and AI platforms involves several areas:

- architecture definition and microarchitecture design focusing on optimising specific performance, power and area targets;
- integration of other silicon IP to complete the chip design, such as memory interfaces, high-speed I/O interfaces, custom accelerators for AI/ML, networking, cache hierarchies and security features;
- verification and simulation to ensure it functions correctly and meets performance targets, and is free of errors;
- physical design including translation from high-level design into a physical layout in geometric data file (GDSII) format involving placement and routing of components;
- tape-out for fabrication; and
- final processes after fabrication including testing and validation alongside system and software development.

The development and implementation of the new high-performance CPU and AI platforms are predicated upon securing access to the ARM CSS and related IP technologies, which are subject to specific qualification criteria.

To expand our product offerings, we plan to enter into joint-development arrangements with technology partners. These partnerships will allow us to tap into their system architecture and software expertise, complementing our silicon IP design and development capabilities. As at the LPD, we have not entered into any arrangements with potential technology partners for the joint development of new high-performance CPU and AI platforms.

The estimated cost for our compute and AI silicon products expansion is approximately RM[●] million for a period of 36 months from the date of our Listing between 2026 and 2029, which will be funded through the gross proceeds from our Public Issue. See Section 4.5 of this Prospectus for further details on the use of proceeds.

7.5.3 Design and develop 2.5D/3D and other silicon products

As part of our strategies and future plans, we target to extend our IC design capabilities to design and develop new 2.5D/3D and other silicon products, addressing opportunities in advanced semiconductor packaging. This includes the following key areas:

(i) CIM silicon dies

We plan to design and develop CIM silicon dies, leveraging our expertise in memory interface IP design and development.

Traditionally, data is stored in memory and transferred to processing units for computation, with the processed data then sent back to memory for storage. This constant data movement often creates bottlenecks, increases latencies and raises power consumption, particularly in data-intensive applications.

To address these challenges, we plan to develop CIM silicon dies that integrate computational capabilities directly within or near the memory chip, utilising the 2.5D/3D chip packaging technologies. This approach eliminates the need for data transfer between memory and processing units, significantly improving performance, efficiency and power consumption. As such, CIM silicon dies are particularly beneficial for applications that require rapid and efficient processing of large datasets, such as AI and machine learning acceleration, as well as high-performance computing workloads.

(ii) I/O chiplets

As part of our new product development plans, we will design and develop 2.5D/3D I/O silicon products to facilitate I/O communications in systems where multiple dies or chips are placed side-by-side on an interposer (2.5D) or vertically stacked (3D).

This includes:

- Memory I/O chiplets, which are designed to facilitate rapid data access between memory stacks and processors. These chiplets can be integrated into larger advanced packages with the high-performance processors, such as those used in high-performance computing and AI, to enable high-bandwidth, low-latency access to memory.
- D2D interconnect chiplets, to provide high-speed connectivity between chiplets using advanced D2D communication standards, such as UCIe, to reduce latency and enable scalable multi-chip architectures.
- Chiplet-based accelerator, which is a custom processing unit designed to perform matrix multiplication, tensor computation, inferencing and cryptographic functions, improving compute core efficiencies and system security.

The I/O chiplets are designed to scale with increasing demand, such as the increase in number of dies in 2.5D/3D advanced packaging. These I/O chiplet silicon products are designed to meet specific power, performance, area and cost requirements.

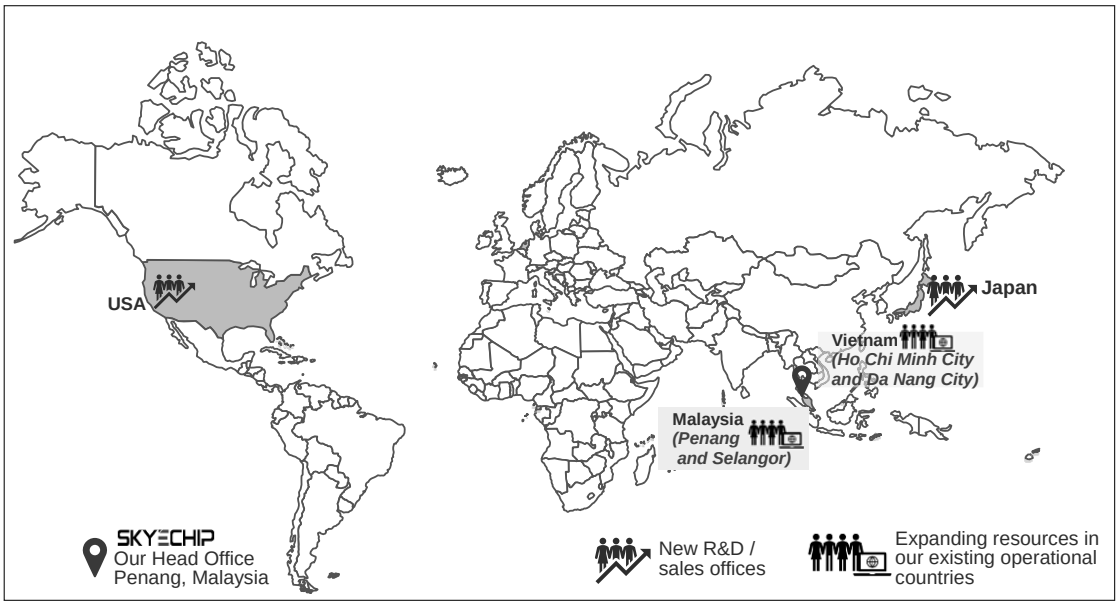
The estimated cost for the design and development of these new 2.5D/3D and other silicon products is approximately RM[●] million for a period of 36 months from the date of our Listing between 2026 and 2029, which will be funded through the gross proceeds from our Public Issue. See Section 4.5 of this Prospectus for further details on the use of proceeds.

7.5.4 Establish and expand facilities and resources

We are scaling up our facilities including setting up new R&D and sales offices to cater to our continuing business and product expansion as well as increasing our technical resources to enhance our capabilities for the design and development of new silicon IPs and products.

7. BUSINESS OVERVIEW *(Cont'd)*

A snapshot of our facility and resource expansion plans is set out below:



(i) Establishment and expansion of R&D and sales offices

We intend to establish and/or expand our R&D and/or sales offices in the following markets progressively between 2026 and 2029:

	2026-2029		2028-2029
	R&D office	Sales office	R&D office
Malaysia	✓		
Vietnam	✓		
Japan		✓	
USA		✓	✓

In December 2024, we commenced our initial operations in Ho Chi Minh City and Da Nang City, Vietnam utilising co-working spaces, and plan to relocate to dedicated offices as we expand our operations between 2026 and 2029. As at the LPD, we have hired 19 technical personnel for our Vietnam operations.

For our domestic operations, we plan to expand our R&D office space in Malaysia between 2026 and 2029 to support our business expansion and product development plans. In addition, we intend to expand our foreign presence by establishing and/or expanding R&D and/or sales offices in Vietnam, Japan and the USA. By securing office space in these markets, we aim to expand our access to local talents, which will enable us to broaden our technical capabilities and market reach, thereby building a stronger regional presence in IC design and development. Additionally, the establishment of sales offices would enable us to provide sales and technical support to potential new customers.

In view of this expansion, we intend to hire personnel across these markets, including sales and technical support teams. These teams will provide pre-sale technical assistance, prepare technical proposals, and generate sales leads to drive our business growth.

As at the LPD, the status of expansion of our operational facilities in foreign markets are as follows:

- we have appointed a sales representative in the USA; and
- we have yet to identify the location for the new offices in the USA and Japan.

(ii) Expansion of computing infrastructure, facilities and software

As part of our facility expansion plan, we will expand our computing infrastructure, facilities and software to support our operations to cater for business and product expansion plans. This expansion includes:

- expansion of computing infrastructure and labs, including servers, cloud services, data storage and network equipment to handle intensive simulation, synthesis and verification tasks. These upgrades will support our complex design works, as well as enabling cloud integration for scalable simulation, verification and data storage, with backup solutions to ensure redundancy.

  This also includes the purchase and/or lease of laboratory equipment such as oscilloscopes for signal integrity and timing analysis, logic analysers to analyse digital signals from prototypes, and pattern generators to generate stimulus patterns for testing silicon IP functions.

- subscription, licensing and/or purchase of EDA and development tools including validation and test tools from multiple providers to support the design and development works.

(iii) Estimated cost for our facility and resource expansion

The estimated cost for our facility and resource expansion is approximately RM[●] million which will be funded through the gross proceeds from our Public Issue, the details of which are set out below:

	Estimated total cost (RM mil)	Timeline for completion
Expand operational facilities and resources	[●]	2026 - 2029
Recruitment and IT infrastructure costs(1)	[●]	2026 - 2029
Expansion of R&D and/or sales offices(2)	[●]	2026 - 2029
Expansion of computing infrastructures, facilities and software(1)	[●]	2026 - 2029
Expansion of computing infrastructure and labs	[●]	2026 - 2029
Subscription, licensing and/or purchase of EDA and development tools	[●]	2026 - 2029
Total	**[●]**	

***Notes**:*

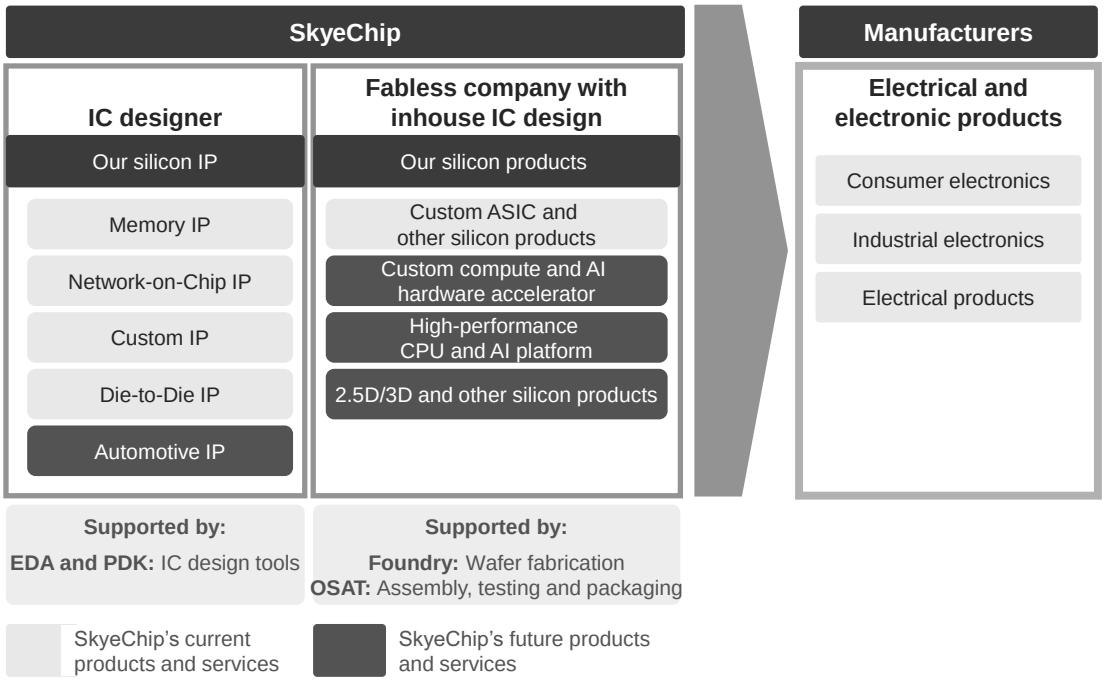
(1) Allocated for our existing operations in Malaysia and Vietnam, as well as new foreign markets including the USA and Japan in future.

(2) Include the rental costs of the R&D and/or sales offices within 36 months from the date of our Listing.

7. BUSINESS OVERVIEW *(Cont'd)*

7.5.5 Our product roadmap at a glance

Since our business commenced in 2020, we have progressed and expanded our product and service offerings to meet the evolving changes in the IC design industry as well as to support our business operations, growth and strategies.



For the Financial Years Under Review, we designed and commercialised several silicon IPs, including memory interface IP, Network-on-Chip IP and D2D interface IP, as well as designed and developed custom silicon IP. In addition, we also designed and commercialised the jointly developed custom ASIC.

From 2026 to 2029, we plan to expand our product portfolio to include automotive IP, custom compute and AI hardware accelerator, high-performance CPU and AI platform, as well as 2.5D/3D and other silicon products, to drive our business growth and increase our revenue base.

See Section 7.7 of this Prospectus for our current products and services, and Section 7.5 of this Prospectus for our future products and services.

7.6 MODE OF OPERATIONS

(i) Silicon IP segment

For the Financial Years Under Review and up to the LPD, our arrangements with customers for the design of standard and custom silicon IPs are primarily based on lump-sum contracts secured. Contracts are secured based on submission of proposals directly to potential customers. Once all technical specifications and commercial terms have been agreed, our customers will then award the contracts.

The payment is in the form of agreed fees based on milestones stipulated in the contracts, which commonly include an initial milestone payment upon signing of the contract. For the Financial Years Under Review and up to the LPD, all revenue from our standard and custom silicon IPs is based on outright sales for the right-of-use of our IP designs.

7. BUSINESS OVERVIEW *(Cont'd)*

Our customers can only use our standard and custom silicon IPs for specific projects as agreed. The use of our standard and custom silicon IPs for different projects will be subject to additional payment and conditions. Our customers commonly have the right-to-use per project and are not allowed to resell and do further development on our standard and custom silicon IPs, while we continue to own the IP rights to the design.

(ii) Custom ASIC and other silicon products segment

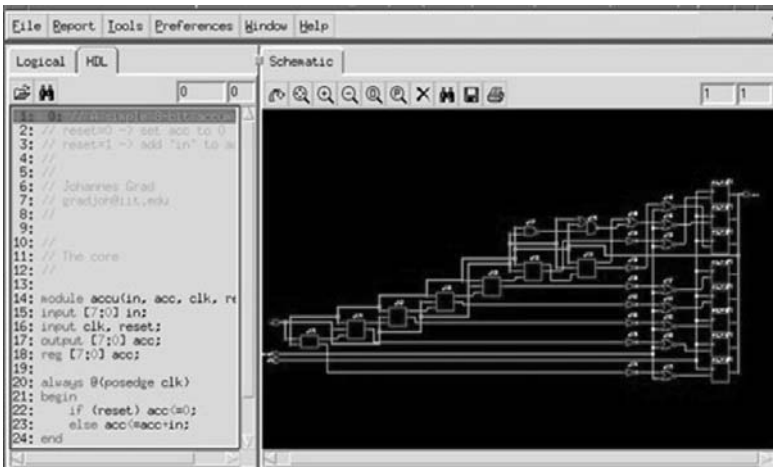
As at the LPD, we have 4 contracts for the design and development of custom ASICs and other silicon products namely RISC-V SoC. Depending on the types of contracts secured, revenue is derived from design and development work completed based on the contracts, as well as product sales based on confirmed purchase orders under cost-plus arrangements.

7.7 PRODUCTS AND SERVICES

7.7.1 Overview

We are an IC design company specialising in silicon IPs, including standard silicon IPs and custom silicon IPs as well as silicon products including custom ASIC.

Part of an IC diagram we would normally design



An IC is a miniature electronic device made up of interconnected transistors, resistors, capacitors and other components etched onto a small piece of semiconductor material, usually silicon. Connections in the context of ICs are conductive paths that allow electrical signals to move between different components and devices on the chip. They enable communications and interactions between various parts of the circuit.

Silicon IP refers to complex pre-designed and reusable functional blocks or modules of circuitry. These blocks can operate as standalone chips or be integrated into larger ICs to perform specific functions, such as processing or communication. Our IPs are pre-designed and pre-verified modules that simplify the design process for chip designers by eliminating the need for extensive design, verification and testing of these functional cores.

The term 'IP' in relation to our IC indicates that we are the original designer and owner of the intellectual property associated with our IC. This allows us to resell or reconfigure our silicon IP for any customer of our choice.

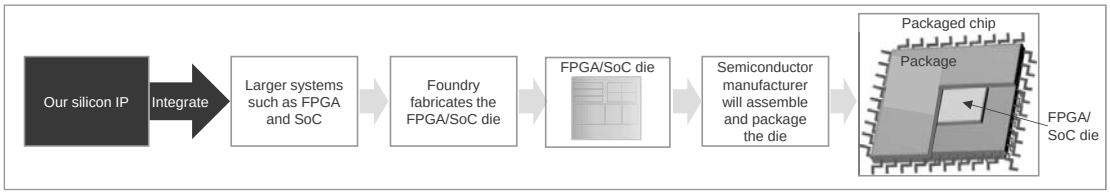
A custom ASIC is a semiconductor chip designed for a specific application rather than for general-purpose use.

7. BUSINESS OVERVIEW *(Cont'd)*

Once we have completed our design of silicon IP, they are compiled into several file formats which are digital formats and may be transmitted over a normal network such as the internet, or stored in a normal data storage device.

Our silicon IPs are commonly integrated with other ICs to form larger systems, such as SoC, CPU and FPGA (a type of functionally reconfigurable IC). These integrated systems are then

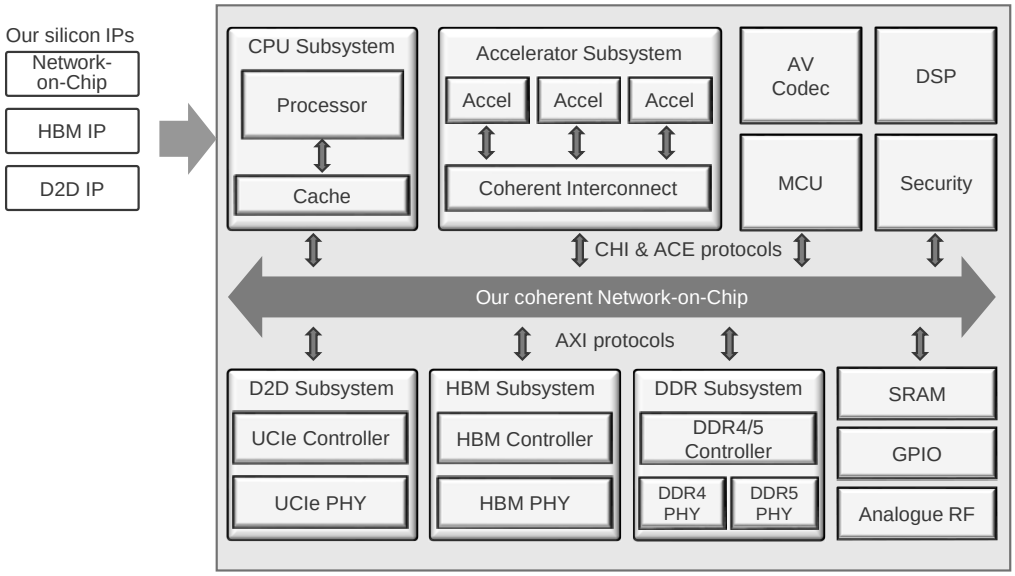
Our position within the value chain of producing a chip



sent to a foundry for IC die fabrication. Finally, the semiconductor company packages the die into a finished chip, which is then assembled onto a motherboard for inclusion into a device.

For silicon IP designs, we undertake comprehensive end-to-end design and development. This process includes system specification; architectural, functional, logic, circuitry and physical design; as well as verification and testing. Our verification process involves simulations, timing analysis and design rule compliance checks. We also develop testbenches and simulation environments to validate the functionality and performance of our IPs.

The following diagram illustrates our silicon IP within a larger processing system:



Note:

HBM = high-bandwidth memory; D2D = die-to-die; Accel = accelerator; MCU = microcontroller unit; DSP = digital signal processing; SRAM = static random-access memory; GPIO = general-purpose input/output; analogue RF = analogue radio frequency; PHY = physical layer

Our technical personnel team is equipped with the know-how of designing silicon IPs and products, with the aid of EDA tools, in advanced process technologies including via PDKs from foundries. EDA tools are software tools that enable us to carry out the design, verification and testing processes, while the PDKs enable us to access technologies from foundries to ensure our IC designs are compatible with the foundry fabrication technologies and processes such as fabricating ICs using process nodes down to 4nm.

We collaborate with EDA tool providers to develop our designs using their tools, such as simulators, modelling systems and logic and physical synthesis tools. Additionally, we participate in final design reviews conducted with customers and foundries to ensure that our IP designs are integrated in line with specified requirements. This process is concluded with the 'tapeout' phase, indicating that our design has been approved and is ready for fabrication into silicon products.

Our technical capabilities are also enhanced by our continuous R&D as demonstrated by our track record of being providers of various memory interface IPs for DDR, LPDDR and HBM. Additionally, our R&D has enabled us to patent our works. As at the LPD, we have 29 patents registered in Malaysia, China and the USA, and 79 patents pending application/registration in Malaysia, China and the USA.

As at the LPD, we have a total of 318 technical personnel including engineers led by our Chief Technology Officer, Teh Chee Hak. Our IC design capabilities include the following:

- **Advanced process node expertise**: We are proficient in designing IP and IC using advanced process nodes down to 4nm, facilitated by access to the relevant PDKs.

- **High-speed memory interfaces**: We have successfully designed and commercialised high-performance memory interfaces such as DDR4/5 with per pin data rate up to 3200 MT/s, LPDDR4x with data rate per pin up to 4267 MT/s, and HBM3 with data rate per pin up to 6.4 Gb/s. Our latest HBM3E is designed to achieve data rate per pin up to 8.0 Gb/s and above.

- **Custom silicon IP development**: We develop custom silicon IPs, tailored to specific application requirements and performance targets, including ASICs.

- **Integration with EDA tools**: We utilise EDA tools to streamline our design process for silicon IP and custom ASIC development.

- **On-chip high-speed interconnects**: We design on-chip high-speed interconnects such as Network-on-Chip architecture for efficient data transfer and integration in complex systems.

- **Precision in timing and signal integrity**: Our design enables high-speed data transfer by addressing timing and signal integrity requirements through precise modelling and simulation, especially in high-speed memory interfaces and Network-on-Chip interconnects.

- **Integration expertise**: Our design enables seamless integration of memory interfaces and on-chip interconnects within multi-processor systems, using our in-house developed integration and configuration software, namely RAPTuner for integration with our Network-on-Chip.

7.7.2 Standard and custom silicon IPs

Our design and development of silicon IP can be broadly categorised into standard and custom silicon IPs as follows:

(i) Standard silicon IP

We design standard silicon IP that adheres to industry specifications, such as JEDEC and UCIe standards. Our standard silicon IPs include memory interface IP, Network-on-Chip IP, and D2D interface IP. See Sections 7.7.3 to 7.7.7 of this Prospectus for further details of memory interface IP and Network-on-Chip IP.

(ii) Custom silicon IP

Custom silicon IPs are typically designed to meet specific performance, power and area requirements, or to offer enhanced or extended features customised to particular customer specifications to ensure optimal integration and functionality for customers' products.

We design and develop custom silicon IPs with the following features:

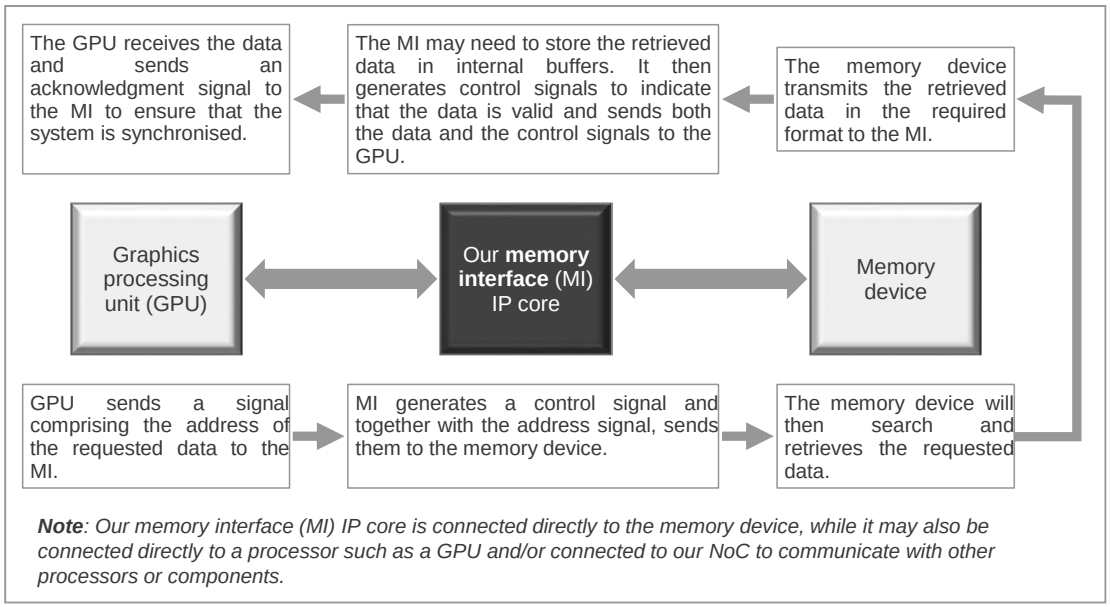
- multi-interface protocols that can support different standards or communication protocols such as DDR and LPDDR memory interfaces, MIPI interfaces, LVDS interfaces and GPIO interfaces. These multi-interface protocols often incorporate bridging mechanisms which enable data to be translated or converted between different protocol types seamlessly, enabling communications across systems (such as CPU, memory and sensors).

- low-power low-latency memory interface features designed to minimise power consumption and optimise memory protocol handling for data flow between compute cores and memory, which are targeted for wearables.

7.7.3 Memory interface silicon IP

We design the IP for the memory interface core. A memory interface core is a specialised module or functional block to facilitate communications between a memory device and a digital logic device.

Illustration of the interaction between our memory interface IP, GPU and memory device



***Note**: Our memory interface (MI) IP core is connected directly to the memory device, while it may also be connected directly to a processor such as a GPU and/or connected to our NoC to communicate with other processors or components.*

Our memory interface IP is crucial in IC design to ensure efficient and reliable communication between the memory and the processing unit or logic device, which affects overall system performance and functionality.

Some of the key functions of our memory interface IP include the following:

- **Protocol handling**: Our memory interface IP implements the specific communication protocols and manages the control and address signals, data transfer and acknowledgements required by various memory types, such as DDR, LPDDR and HBM interfaces.

7. BUSINESS OVERVIEW *(Cont'd)*

- **Data buffers**: Our memory interface IP uses data buffers to temporarily store data for synchronisation between the processor and memory, as well as to reorder data for more efficient processing.

- **Timing management**: Our memory interface IP manages clock signals and timing parameters for read (data retrieval) and write (data storage) operations to synchronise these actions and avoid conflicts or out-of-sequence read/write operations.

- **Error correction**: Our memory interface IP also includes error detection and correction capabilities (such as error correction code) to ensure reliability and data quality during data transfers.

- **Power management**: Our memory interface IP often incorporates power management features to optimise energy consumption, particularly important in mobile and embedded applications.

- **Configuration and initialisation**: Our memory interface IP typically includes functions for configuring and initialising memory devices, ensuring that they are correctly set up correctly and trained before use.

Our memory interfaces are used for the following applications:

- **Memory and CPU interface**: This is the most common application, where memory interfaces connect the system's memory (random-access memory) to the CPU. This ensures data and instructions are efficiently transferred between these components.

- **Memory and GPU interface**: In systems with a GPU, memory interfaces connect the GPU to its dedicated memory such as HBM. This is essential for high-bandwidth data transfer required for graphics processing.

- **Memory and other accelerators**: Memory interfaces are used to connect memory to other accelerators, such as DSPs, network interface controllers or custom hardware accelerators. This helps in offloading specific tasks from the CPU and improving overall system performance.

- **Memory and network interfaces**: For high-performance networking applications, memory interfaces may connect to network traffic management ASICs or other network components, facilitating high-speed data transfer and buffering.

- **Inter-processor communication**: In multi-processor or multi-core systems, memory interfaces can be used to facilitate communication between different processors or cores. This includes sharing data between processors in a multi-core CPU or between different chips in a SoC.

- **Memory hierarchies**: In complex systems, memory interfaces help manage various levels of memory hierarchy, such as cache memory, main memory and off-chip memory. Efficient interfaces are crucial for maintaining optimal performance across these different memory hierarchy levels.

Our memory interface IPs adhere to JEDEC standards to ensure interoperability and reliability, focus on increased data rates for faster data transfers, power efficiency optimisation and maintaining signal integrity.

Our memory interface IPs are pre-designed and pre-verified, which enables us to either resell it as-is or quickly reconfigure it for use in different applications and for different customers instead of designing the memory interface core from scratch.

7. BUSINESS OVERVIEW *(Cont'd)*

Our memory interface IP also operates through a memory interface IP firmware, in which the development is carried out in-house. This firmware is crucial for ensuring the functionality, efficiency and compatibility of our memory interface IP with various memory technologies and suppliers. Some of the functionalities of the firmware that we develop include the following:

- Perform initialisation, configuration and training sequences to initialise and configure the memory device.

- Performance optimisation including timing analysis to ensure that the memory interface meets the required timing constraints, and to optimise the design to achieve the desired throughput and latency metrics.

- System compatibility to ensure that the memory interface integrates smoothly with other IPs in the system such as CPU and GPU.

- Power management to optimise power consumption of the memory interface, and to handle low-power modes and power-saving features.

Our comprehensive memory interface IP integrates multiple functionalities, including a memory controller IP and PHY IP as follows:

- **Memory controller IP**: The memory controller IP is designed to manage communication between the memory subsystem and processor or other system components. It handles the logical operations required to read from and write to the memory according to the specific memory standard in use. This involves translating the processor's requests into appropriate commands for tasks such as initialisation, refresh, power-down, error correction and data flow management.

  The design of the memory controller IP incorporates the following considerations and parameters:

  - Command sequencing: Converts memory commands from the processor into sequences of commands suitable for the memory device. This includes managing the proper sequencing and timing of commands to ensure correct operation.

  - Address translation: Maps virtual addresses used by the processor to physical addresses in the memory device. This ensures that data is correctly located and accessed.

  - Data path management: Manages the data path for read and write to ensure data integrity and proper timing. This involves designing data queues that support the transfer of data signals between the controller and the memory devices. The number of data queue lines varies depending on the memory type and configuration.

  - Timing control: Ensures that memory operations adhere to timing constraints specified by standards such as DDR5 and HBM3. This includes managing signal timing to meet performance requirements.

  - Error correction: Implements error detection and correction algorithms to maintain data integrity and reliability. This ensures that data errors are detected and corrected as needed.

  - Power management: Incorporates features to reduce energy consumption, especially during idle periods, to enhance overall power efficiency.

7. BUSINESS OVERVIEW *(Cont'd)*

- **PHY IP**: The PHY IP is designed to manage the physical data transmission, handling the electrical and timing characteristics required for the connection between the processor and memory devices. It converts digital signals from the memory controller into the appropriate physical signals for the memory device. This ensures that electrical signals are accurately converted and timed to maintain reliable and high-speed data transfer.

  The design of the PHY IP incorporates the following considerations and parameters:

  - Signal integrity: Ensures minimal distortion and noise during signal transmission, maintaining high-quality data transfer.

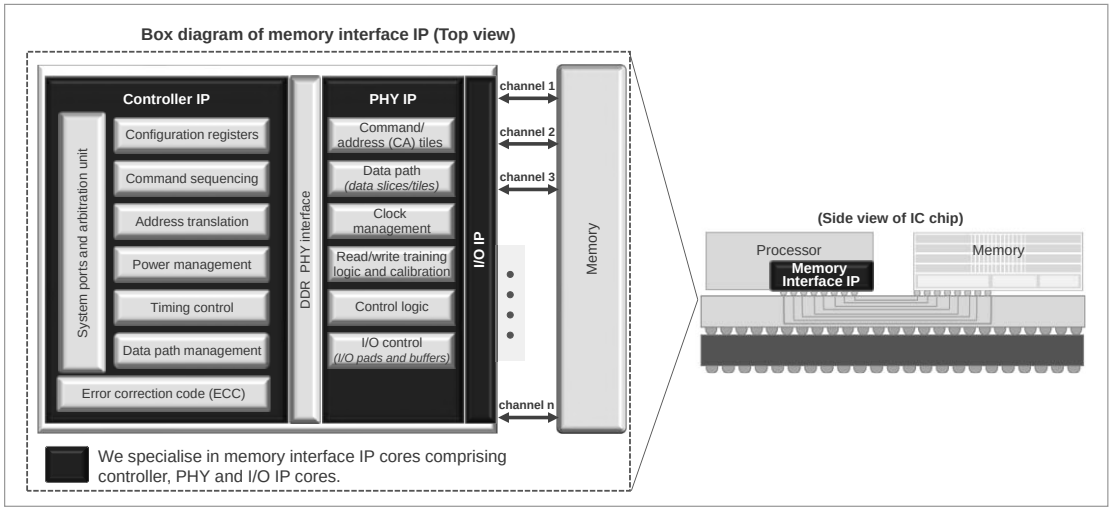
  - Timing calibration and management: Provides precise timing control to meet the stringent requirements of high-speed memory interfaces, ensuring accurate data transmission.

  - Interface standards: Adheres to physical interface standards based on the memory technology used, such as DDR, LPDDR or HBM. This ensures compatibility with various memory types and configurations.

  - Calibration: Maintains optimal signal integrity and performance through calibration processes. This includes data serialisation and deserialisation, converting parallel data from the memory controller into a serial form for transmission, and then converting it back to parallel form upon reception.

  - I/O management: Manages physical input and output pins that connect memory to other system components. It handles the actual connections to the memory, including driving and receiving signals at the required voltage levels. The design incorporates features for electrostatic discharge protection, adherence to I/O standards, and power distribution management. This ensures that signals are properly driven and received, facilitating reliable physical transmission and reception of data.

A box diagram to illustrate the memory interface IP we designed is depicted below:



n = number of channels

7. BUSINESS OVERVIEW *(Cont'd)*

We can design memory interface IP across a range of process nodes down to 4nm. For the Financial Years Under Review and up to the LPD, we have developed the following memory interface IPs that are licensable to customers:

Memory interface IP						
	LPDDR4	**LPDDR4x**	**LPDDR5**	**LPDDR5x**	**HBM3**	**HBM3E**
Memory controller	√	√	√	√	√	√
PHY	√	√	√	√	√	√

7.7.4 DDR and LPDDR memory interface IP

DDR and LPDDR memory interface IPs are specially designed to facilitate efficient communication between processors and their respective DDR or LPDDR memory modules. These IPs ensure compliance with the performance and reliability standards required by each memory type. DDR memory interface IPs are optimised for high data transfer rates, while LPDDR memory interface IPs offer the additional benefit of lower pin count and lower power consumption, making them ideal for energy-efficient applications. Both DDR and LPDDR memory and their corresponding interface cores are used in a range of applications, including general computing, networking equipment, embedded systems and consumer electronics.

We have successfully commercialised various versions of our DDR and LPDDR memory interface IPs including the memory controller and PHY with the following features:

- data rate and bandwidth that support data rate per pin up to 8533 MT/s and above for LPDDR5x to meet the requirements of both mobile and server memory standards;

- latency management optimised to improve performance by minimising delays in data access and transfer;

- channel configurations capable of single-channel, dual-channel or multi-channel configurations to enhance bandwidth based on application needs;

- error correction code to detect and correct data transfer errors for DDR types;

- initialisation featuring automated initialisation sequences during startup for streamlined operation; and

- power management including power-saving features such as power-down modes, dynamic frequency switching and self-refresh to reduce power consumption when the memory is not actively in use.

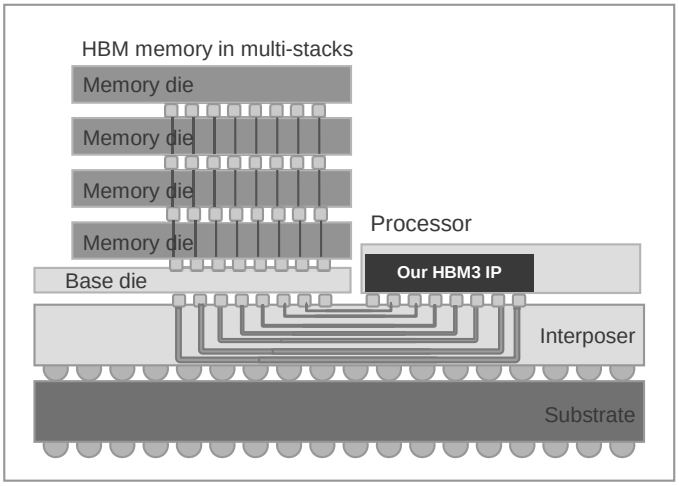
Some of the features and typical performance of our standard LPDDR memory interface IPs include:

Memory Interface IP	Max data rate per pin	SDRAM mode support	Common applications
LPDDR4	3200 MT/s	x8, x16	Optimised for lower power consumption, this solution is ideal for mobile and power-critical applications such as smartphones, tablets, wearable devices, IoT devices, and other consumer electronics. It is also well-suited for deploying AI applications.
LPDDR4x	4267 MT/s	x8, x16	
LPDDR5	6400 MT/s	x8, x16, x32	
LPDDR5x	8533 MT/s and above	x8, x16, x32	

7. BUSINESS OVERVIEW *(Cont'd)*

7.7.5 HBM interface IP

HBM is a type of high-speed memory designed to provide significantly greater bandwidth compared to traditional DRAM. Our HBM interface IP is optimised to handle these higher data transfer rates, ensuring efficient communication between processors and HBM devices. It also ensures compliance with the performance and reliability specifications set by HBM standards. HBM devices and their interfaces are used in applications such as AI, machine learning, data centres and high-end graphics cards, where large volumes of data need to be processed and rendered efficiently and speedily.



Through our R&D efforts, we began with the HBM3 controller and PHY IP in 2022 and have continued to innovate, and commercialised the new HBM3E interface IP in 2024. These technological advancements reflect our ongoing commitment to increasing memory interface bandwidth and enhancing overall system performance to meet the growing demands of high-performance computing, AI, and data-intensive applications.

Our HBM interface IPs are designed to facilitate high-speed data communication between a host system (such as an FPGA or SoC) and multi-stack HBM modules within a packaged semiconductor device.

We specialise in designing the HBM interface IP with the following features:

- **interface management** to manage data transfer between the host system and memory device to ensure data integrity and proper timing;

- **clock management** to generate and manage clock signals for the HBM memory interface, ensuring synchronisation between the controller and memory. This includes timing calibration to guarantee reliable data transfer;

- **protocol handling** to oversee command scheduling to optimise the order and timing of memory access commands for maximum throughput, and manage data transactions according to the HBM protocol;

- **power management** to optimise power consumption based on the operational state and workload, featuring dynamic power adjustment to meet performance requirements; and

- **additional features include** error detection and correction mechanisms to ensure data integrity and reliability, performance monitoring of the memory system, memory initialisation sequences on power-up or reset, execution of training sequences for signal timing calibration, and configuration, monitoring and debugging features to support system integration.

We have successfully taped out two HBM interface IP designs that support data rates up to 9.6 Gb/s. These designs utilised stacked DRAM dies connected to a very wide 1024-bit bus interface, following JEDEC standards.

7. BUSINESS OVERVIEW *(Cont'd)*

The typical features and performance of our HBM interface IP are as follows:

HBM Interface IP	HBM3	HBM3E
Maximum data rate per pin	6.4 Gb/s	8.0 Gb/s and above
Memory bus interface width	1024-bit	1024-bit
Bandwidth per stack (memory throughput) (1)	819 GB/s	1024 GB/s and above

***Note**:*

(1) Assuming 1024-bit data bus interface width.

7.7.6 Network-on-Chip IP

In 2021, we began our design and development of Network-on-Chip IP, specifically for coherent Network-on-Chip IP to enhance communication and data flow across various components and subsystems within a SoC. In 2022, our coherent Network-on-Chip IP was licensed to a major customer.

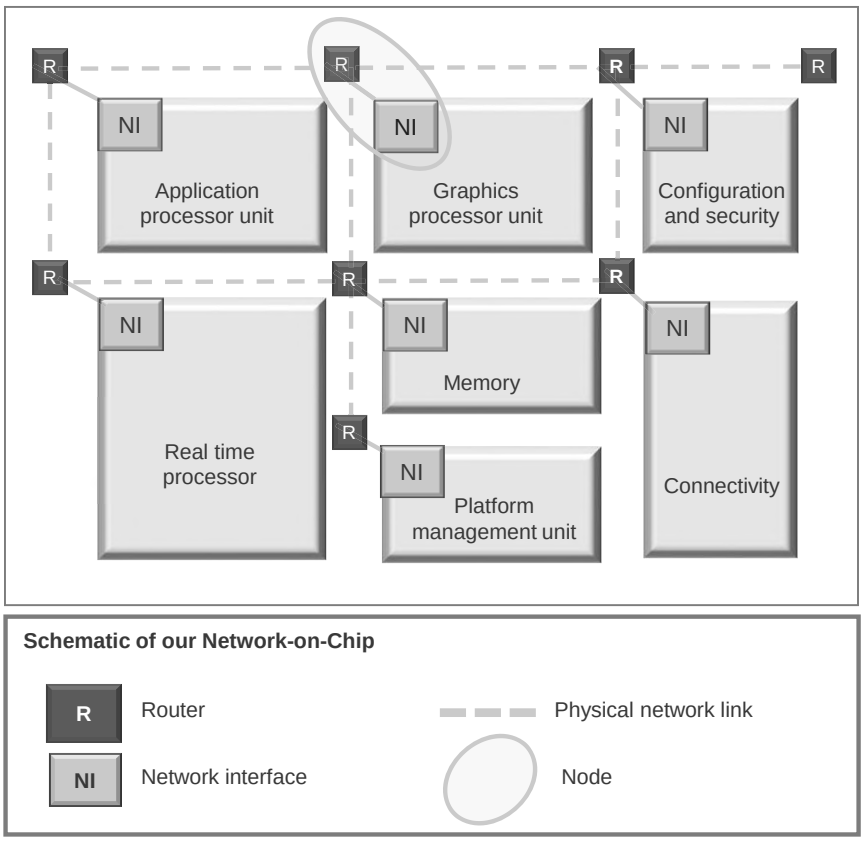
The primary function of Network-on-Chip IP is to manage and optimise communication between different components within a chip such as a SoC, CPU and FPGA. This IP provides the essential infrastructure for efficient data transfer, signal routing and connectivity among components or subsystems within a chip.

Our Network-on-Chip IP architecture links various components and subsystems, including processors, memory, AI accelerators, security components and other I/O components, to enable seamless communication between them. Our coherent Network-on-Chip IP addresses specific performance, power efficiency and area requirements, and is employed in a range of applications in computing, AI and communications.

We use a router-based Network-on-Chip architecture, which employs smart routers to manage and facilitate communication between various components, subsystems or cores. This approach reduces wire routing congestion, enhances performance and optimises power consumption to meet targeted functional and performance specifications. The primary design elements of our Network-on-Chip IP include routers, network interfaces and physical links as illustrated in the diagram below:

7. BUSINESS OVERVIEW *(Cont'd)*

Block view of our Network-on-Chip IP



Schematic of our Network-on-Chip

- A router's primary function is to receive data and transmit it through the Network-on-Chip to its intended destination. The router is connected to both its network interface and the overall Network-on-Chip.

- A network interface is attached to a processor, memory or other subsystem or core. When a subsystem needs to send data to another subsystem, the network interface encapsulates the data into packets, formats them according to the Network-on-Chip protocol, and then hands over the formatted data packets to the router for transmission over the Network-on-Chip to the destination node.

- The physical links which represent the network pathway, connect routers and network interfaces to facilitate communication between nodes and subsystems.

Our routers are "smart routers" having the following features:

- quality of service to prioritise different types of traffic to ensure optimum performance and reliability;

- fault tolerant to handle and recover from faults or failures within the network; and

- traffic management using advanced algorithms for load balancing and congestion management.

7. BUSINESS OVERVIEW *(Cont'd)*

Our Network-on-Chip IP design and development cover various aspects including among others:

- **Topology creation**: This involves defining the arrangement of nodes and their connections within the network. Each node typically includes a router, which is responsible for managing data routing. These routers are interconnected in a network that facilitates communication with other routers in the system, enabling efficient data exchange across the entire Network-on-Chip.

- **Routing algorithm**: This involves determining the paths for data packet movement across the network. Algorithms can be deterministic or adaptive, affecting latency and throughput. Our routing algorithm is traffic aware and optimises for maximum throughput with low latency.

- **Flow control mechanism**: This involves managing data packet transmission to prevent congestion and data loss.

- **Quality of service**: This involves mechanisms to prioritise certain types of data traffic, ensuring efficient data transfer minimising latency and managing varying data flow requirements.

- **Bandwidth**: This includes link bandwidth and overall network throughput, which determine the data transfer rate.

- **Interconnect link design**: This covers the physical and electrical properties of links, including width, signalling and clocking techniques, and error detection/correction capabilities.

- **Buffering**: This involves the size, allocation and management of router buffers. Buffering impacts latency and congestion handling, with minimal latency being critical for high-performance applications.

Our Network-on-Chip architecture offers several key advantages over traditional interconnects, such as bus-based, point-to-point, hierarchical and cross-bar switches. These advantages make Network-on-Chip a popular choice for modern SoC designs, especially in systems with high complexity and performance demands.

Some of the benefits of Network-on-Chip architecture over other traditional interconnects include the following:

- **Scalability**: It uses routers and switches, which facilitate easy expansion by adding more nodes. This modular approach allows for increased scalability with minimal impact on overall system complexity, as new nodes can be integrated into the network without significantly disrupting existing connections or requiring major redesigns.

- **Performance**: It employs our proprietary routing algorithms and parallel communication to provide high performance and efficient use of bandwidth. It uses packet-based communication, which helps in managing and directing traffic more effectively compared to shared bus architecture. This reduces the risk of congestion and improves overall system performance.

- **Modularity**: The modular nature of Network-on-Chip facilitates ease of integration and reconfiguration.

- **Flexibility**: Able to customise topology, routing algorithms and network parameters to suit different applications.

- **Power efficiency**: It optimises data routes to reduce power consumption.

7. BUSINESS OVERVIEW *(Cont'd)*

In addition, we have our in-house developed proprietary software to support the integration and configuration of our Network-on-Chip IP into our customer's ICs. Our proprietary software is typically packaged with our Network-on-Chip IP for use by our customers. Our Network-on-Chip IP integration and configuration software, namely RAPTuner, is a system optimisation tool that facilitates system modelling and performance analysis to enhance interconnect and memory performance. It is designed to integrate seamlessly with our memory interface IP and Network-on-Chip IP, which works in conjunction with other subsystem IP models.

Our Network-on-Chip IP encompasses both coherent and non-coherent Network-on-Chip IP, designed for high bandwidth, low power consumption and reduced latency in multi-processor semiconductors. They offer flexible configuration and reliable functionality.

- **Coherent Network-on-Chip IP**

  Coherent Network-on-Chip IPs are specialised interconnect designs that manage the coherence or consistency of data across different caches or memory locations in a multiprocessor or multi-core environment such as SoC or a multi-core CPU. Coherence ensures that all processors or cores in a system have a consistent and up-to-date view of shared data.

  To maintain data consistency across multiple nodes within the network, the following design considerations are implemented:

  - **Coherence protocols**: Our Network-on-Chip IPs adhere to standards such as AXI Coherence Extension (ACE) and Coherent Hub Interface (CHI) protocols to ensure interoperability and correctness. These protocols provide necessary coherence mechanisms, scalability and efficiency enhancements.

  - **Data path optimisation**: Focuses on pipeline design to ensure data and control signals propagate through the network within the clock period, achieving the desired operating frequency. By decoupling transactions, the network can handle multiple outstanding transactions simultaneously to maximise throughput.

  - **Latency management**: Minimises the number of intermediate nodes that data packets traverse by implementing efficient arbitration mechanisms to prioritise high-traffic operations and maintain low latency for critical tasks.

  - **Power efficiency**: Incorporates dynamic power management techniques such as clock gating and power gating to manage power consumption. Additionally, thermal management features are included to handle the heat generated by high-frequency operations, ensuring reliable performance.

- **Non-coherent Network-on-Chip IP**

  Non-coherent Network-on-Chip IPs are designed to provide efficient communication infrastructure within an SoC without maintaining data coherence across multiple caches. This focuses on efficiently routing data between nodes across the Network-on-Chip, prioritising high bandwidth, low latency and flexibility to meet performance specifications. Key functions in our designs include data routing, traffic management, topology configuration, protocol translation and power management.

  Our non-coherent Network-on-Chip IP designs utilise simpler and more flexible protocols compared to coherent Network-on-Chip IP. We commonly use Advanced eXtensible Interface (AXI), Advanced Peripheral Bus (APB) and Advanced High Performance Bus (AHB) protocols to support high-bandwidth data transfers across various applications.

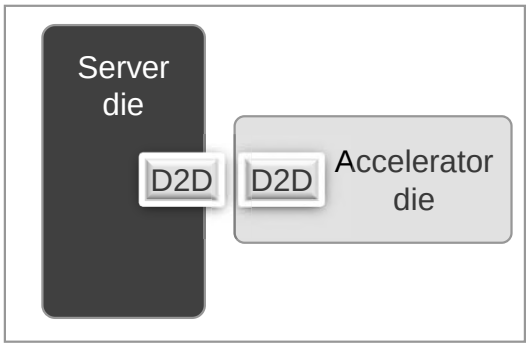
7. BUSINESS OVERVIEW *(Cont'd)*

7.7.7 Die-to-die interface IP

We developed and commercialised a new standard silicon IP, namely D2D interface IP in July 2025, to facilitate high-speed communication between different functional blocks within a multi-die package, such as a CPU, GPU and FPGA, or other processors configured in 2D, 2.5D or 3D structures.

The design and development will include both the controller and PHY block to facilitate connections between the interconnect layers across multiple dies. This will optimise power, performance (including latency and bandwidth) and area to enable efficient inter-die connectivity for a wider range of applications.

Our D2D interface IP



D2D interface IPs are used in a variety of applications, including the following:

- high-performance computing: D2D interface IP enables the integration of CPUs with accelerators such as GPUs or FPGAs, by combining the pre-designed and pre-verified chiplets to optimise power, performance and time-to-market, which are ideal for advanced computing systems;

- data centres: D2D interface IP supports the co-packaging of different dies within server systems, improving bandwidth and reducing latency for networking and storage applications, which enhance the efficiency and scalability of data centre operations;

- AI and machine learning: D2D interface IP facilitates high-bandwidth communication between specialised accelerators, CPUs, and memory. D2D interfaces are essential for scaling the processing of large datasets, reducing latency and increasing bandwidth, thereby significantly enhancing the performance of AI and machine learning workloads; and

- networking equipment: D2D interface IP enables the connection of multiple processors or FPGA dies, providing the high-bandwidth, low-latency communication necessary for compute-intensive applications in networking.

The D2D interface IP will comply with the UCIe protocol, which is designed for multi-module interconnections at speeds up to 2048 Gb/s per module. This compliance ensures interoperability and ease of integration.

This new D2D interface IP is designed for chiplet-based architectures, enabling efficient communication between chiplets within a single package. It supports connectivity between components such as CPUs, GPUs and memory modules, which meet the high-speed, low-latency requirements of multi-die packages. The key applications include high-performance computing, data centres, advanced computational systems for AI, and networking equipment.

7.7.8 Silicon products

7.7.8.1 Custom ASIC

We leverage our expertise in silicon IP to expand into the design and development of custom ASIC. A custom ASIC is a semiconductor chip designed for a specific application rather than for general-purpose use.

7. BUSINESS OVERVIEW *(Cont'd)*

This is to address business opportunities in emerging trends that require silicon products specifically designed and optimised for power efficiency and high performance. These segments include mobile communications, AI, high-performance computing, data centres and future automotive applications. Our portfolio of silicon IP and access to advanced process nodes down to 4nm provides us with a strong foundation for designing and developing new custom ASIC products.

Custom ASIC products are engineered to perform specific functions, offering enhanced efficiency in power consumption and performance, reduced physical footprint and the capability to execute proprietary algorithms that standard devices cannot perform efficiently.

The development process involves defining specifications, architecture definition, creating detailed designs and verification of the designs. We utilise design tools and software for simulation and verification before proceeding to prototype creation, testing, refinement and ultimately mass production.

Designing and developing custom ASIC products represent a new business activity for us. We have been focusing and will continue to focus on designing IPs and ICs that are combined with other third-party IPs to create complete chips or SoCs.

(a) IoT ASIC

The design of the IoT ASIC leverages our silicon IPs namely memory interface IP and Network-on-Chip IP. This IoT ASIC is a specialised IC designed to optimise for edge AI computing applications such as robotics, industry IoT devices, AI learning systems and secure access systems.

Some of the key design consideration features include:

- minimise power consumption;
- performance enhancement such as accelerated inference;
- reduce latency; and
- enhanced security.

As at the LPD, we have 2 contracts with a customer to jointly develop IoT ASICs with the incorporation of our silicon IP. Our IoT ASIC products integrate our memory interface IP and Network-on-Chip IP with our partner's proprietary IPs. Both of these IoT ASICs are built on a 7nm process technology.

As at the LPD, the development status and launch timeline of our two IoT ASICs are as follows:

IoT ASIC	**1st IoT ASIC (1)**	**2nd IoT ASIC (3)**
Initial design and development	√	√
Tapeout	√	√
Creation of mask set	√	√
Creation of prototypes	√	√
System and software development (2)	√	On-going
Pilot run and mass production (2)	√	On-going
Completion/expected completion	2024	end-2025

Notes:

(1) The prototypes were completed in September 2024. We have commercialised this IoT ASIC in September 2024 with the sales of products.

(2) These were carried out by our technology partner.

7. BUSINESS OVERVIEW *(Cont'd)*

(3) The prototypes were completed in April 2024.

Both of IoT ASIC project tapeouts were completed and the mask sets were created in 2024 after the ASIC design was fully verified and validated to meet all design specifications, rules and checks. The tapeout process generates the final design file used to create the mask set.

A mask set consists of a series of photomasks or photographic plates used in the photolithography process. Each photomask represents a specific layer of the ASIC. We are supported by a foundry in Taiwan, which is involved in wafer and die fabrication.

The prototypes for both IoT ASICs were completed in 2024 and samples of the packaged chips have been fabricated. The prototypes underwent a series of evaluations, including functional testing to confirm that the ASIC products perform their intended tasks effectively. The prototypes were integrated into the system board, and the system and software development will be carried out by our technology partner.

(b) Custom AI inference ASIC

Custom AI inference ASIC is a component within an AI system designed to work with a pre-trained AI model to make inferences or predictions based on new data inputs. During the training phase, the AI model learns from large amounts of data to identify patterns and relationships. Once the data is trained, the model is deployed onto the custom AI inference ASIC, utilising the trained AI model to apply those patterns and relationships to new data and generate predictions or make decisions.

The custom AI inference ASIC is designed to optimise the inference phase of AI models, enhancing both processing speed and power efficiency. The new custom AI inference ASIC is designed for on-premises AI inference scalable applications. On-premises scalable applications refer to software systems or platforms that are deployed locally within an organisation's hardware and infrastructure, such as desktops, servers and data centres. Some of the examples of on-premises AI inference scalable applications are AI inference systems for real-time decision-making, large-scale data analytics platforms or video surveillance systems with AI-based analysis for security monitoring.

An AI inference is a purpose-built product designed to accelerate specific AI workloads by improving computational efficiency. The architecture of this custom AI inference is optimised for AI algorithms and data structures, aiming to achieve high performance in both processing speed and power efficiency. It is tailored to accelerate operations critical to neural networks, such as matrix multiplication, convolution and other mathematical functions.

Neural networks often use matrix representations, where matrix operations are essential for many AI tasks. This chip can be designed to handle various AI workloads, including image recognition, speech recognition and natural language processing. For example, in image recognition, a neural network performs multiple matrix multiplications between an input image and learnt data matrices to produce a final classification output. Similarly, in machine learning, matrix multiplication is a key operation in algorithms where computations on weight matrices are performed. During training, the network learns to map input data to the desired output. Once trained, the network can be used for inference to classify new input data. Training and inference require different processing parameters in terms of memory bandwidth and computational needs. As at the LPD, we have a subsisting contract with a customer for the development of custom AI inference ASIC.

7. BUSINESS OVERVIEW *(Cont'd)*

7.7.8.2 Other silicon products - RISC-V SoC

RISC-V SoC is a type of silicon products with the incorporation of RISC-V processor cores integrated with various silicon IPs including our Network-on-Chip IP and other third-party silicon IPs. RISC-V is an open-standard Instruction Set Architecture (ISA) defines how a processor works at the instruction level such as how it loads data or control program flow. As at the LPD, we secured a contract with a customer for the development of RISC-V SoC incorporating our Network-on-Chip IP in September 2025.

7.7.9 Others segment

Our other business activities include providing design services as part of our integrated customer support services, as well as design of memory test systems.

Leveraging our expertise in silicon IP design, we also offer customised design services to meet specific customer requirements. This enhances the adaptability and performance of our IP across various applications. Our services support the seamless integration of silicon IP into system designs, ensuring compatibility and functionality. This helps our customers accelerate product development cycles and efficiently deploy new technologies.

In addition, we have also completed several designs of memory test systems based on customers' requests.

7.7.10 On-going and secured contracts

As at the LPD, we have 12 on-going projects for our silicon IPs and custom ASIC. The total project value amount to approximately RM153.7 million, of which the unbilled order book is approximately RM37.4 million as at the LPD. For avoidance of doubt, this amount does not include potential revenue from the sale of silicon products.

7.8 MAIN OPERATIONAL FACILITIES

As at the LPD, the details of our main operational facilities are as follows:

	Main function	Built-up area (in square metres unless otherwise stated)	Location of facility
SkyeChip[(1)]	Head office	608	1-18-12 Suntech @ Penang Cybercity Lintang Mayang Pasir 3 11950 Bayan Baru Pulau Pinang
	Office	792	1-17-01 Suntech @ Penang Cybercity Lintang Mayang Pasir 3 11950 Bayan Baru Pulau Pinang
	Office	6,867 sq ft	1-17-02 Suntech @ Penang Cybercity Lintang Mayang Pasir 3 11950 Bayan Baru Pulau Pinang
	Office	1,903	1-20-01 Suntech @ Penang Cybercity Lintang Mayang Pasir 3 11950 Bayan Baru Pulau Pinang

7. BUSINESS OVERVIEW *(Cont'd)*

	Main function	Built-up area (in square metres unless otherwise stated)	Location of facility
	Office	7,660 sq ft	No. 3F-1&2, 3rd Floor Tower 4 @ PFCC Jalan Puteri 1/2, Bandar Puteri 47100 Puchong Selangor Darul Ehsan

Note:

(1) We occupy an office in the Silicon Research & Incubation Space under the Penang Silicon Design @5km+ initiative by the State Government of Penang where we enjoy the use of certain facilities and services for our IC design activities. In addition to our Malaysian operations, we utilise co-working spaces located in Ho Chi Minh City and Da Nang City, Vietnam as at the LPD.

7.9 MACHINERY AND EQUIPMENT

We are involved in IC design, supported by hardware and software comprising computers, servers and peripherals, with a net book value of RM3.5 million as at 31 March 2025. In addition, we also have engineering tools for our custom ASIC, with a net book value of RM27.4 million as at 31 March 2025.

7.10 PRODUCTION CAPACITY AND UTILISATION

Operational capacity, output and utilisation rate do not apply to our silicon IP and custom ASIC design operations as the nature of our business is based on providing services. We do not depend on the use of machinery and equipment, except for general computing equipment, to provide these services.

7.11 BUSINESS PROCESS FLOW

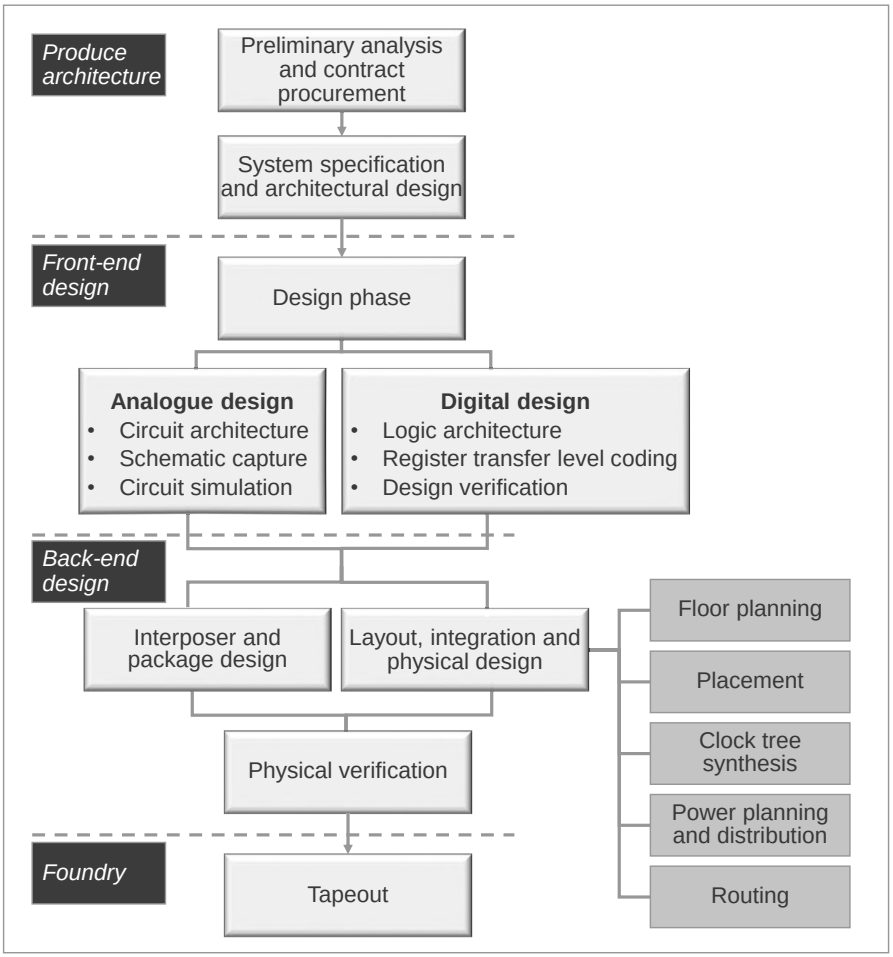
7.11.1 Design and development of silicon IP

We carry out end-to-end design and development work for silicon IPs, specialising in memory interface IP and Network-on-Chip IP for our customers. Our design and development process supports both first-time development of standard and custom silicon IPs tailored to individual customer needs.

For standard silicon IPs, we design and develop IPs based on industry standards such as JEDEC and UCIe, supported by our continuous research and development effort. Our standard silicon IPs are fully configurable, allowing us to customise them to meet each customer's specific needs while ensuring compliance with relevant industry standards. For custom silicon IPs, we design and develop IPs based on unique specifications provided by our customers, ensuring that the IP meets their technical and functional requirements.

7. BUSINESS OVERVIEW *(Cont'd)*

Our business process flow for the design and development of silicon IP for our new customers is depicted below:



Preliminary analysis and contract procurement

Our business operation commenced upon receiving an expression of interest from a prospective customer. Our business development personnel will engage with the customer to understand their needs. We will determine whether to use standard silicon IPs, develop a new custom silicon IP or enhance an existing core design to best address their needs.

Based on the gathered information, we will develop a proposal outlining our proposed solution, project scope, timeline and fee quotation. If our proposal receives initial acceptance, we will fine-tune our proposal after further discussions, resulting in a final proposal ready for customer acceptance.

7. BUSINESS OVERVIEW *(Cont'd)*

System specification and architectural design

Upon securing a contract, we will conduct a detailed user requirements study to establish a comprehensive system specification. This process translates customer needs into detailed technical requirements, including functionality, performance, power consumption, complexity and chip size parameters. The system specification is provided to our customer for further fine-tuning and approval.

Subsequently, our architectural design phase will commence based on the agreed system specification. This involves defining the IP's overall circuit structure, components and required functional blocks, creating a blueprint for subsequent design stages. The specific function blocks vary depending on the IP's functionality. Some common functional blocks include:

- register structures: to store data temporarily;
- control units: to coordinate the operations across the design blocks;
- I/O interfaces: to connect the IP to external systems;
- clock and reset circuits: to provide timing and synchronisation;
- data path: for routing data between components;
- configuration structures: to manage the functionality of various design blocks; and
- test structures: to test the design for debugging and manufacturing.

Design phase

We primarily use two types of designs for different applications, namely analogue and digital. Analogue designs are mainly used for signal processing, such as sound, audio and radio frequency transmissions, while digital designs are mainly used for data processing in discrete form, often represented as binary.

Analogue design

We begin our analogue design by developing a top-level architecture that meets the required specifications to establish the overall circuit architecture. This is followed by creating device-level circuit descriptions using components such as transistors, resistors and capacitors to support the design. EDA tools are used to capture the circuit as a schematic. We then use simulation tools to analyse the circuit's behaviour under various conditions, identifying and rectifying potential issues early in the process.

Digital design

We begin our digital design by modelling the circuit's functionality, structure and data flow using register transfer level design to establish the logic architecture. This involves decomposing the circuit into smaller and manageable sub-modules, represented in hardware description languages such as Verilog. Next, the register transfer level design is synthesised into a gate-level netlist through logic synthesis, optimising for power, performance and area. We use EDA tools to automate this process, generating a netlist that specifies logic gates and their interconnections.

Additionally, we implement design-for-test techniques by incorporating additional features such as scan chains, built-in self-test and boundary scan cells to facilitate testing and debugging of both analogue and digital components, ensuring design accuracy and timing integrity. Logic verification is also performed as part of design verification, ensuring the design's functionality against its specifications before physical implementation. This process uses simulation, formal verification and verification IP to ensure the design operates correctly across various input scenarios.

Layout, integration and physical design

Our technical personnel will design the physical implementation of the analogue circuitries, followed by integration of both analogue and digital circuit blocks into a single and cohesive layout database.

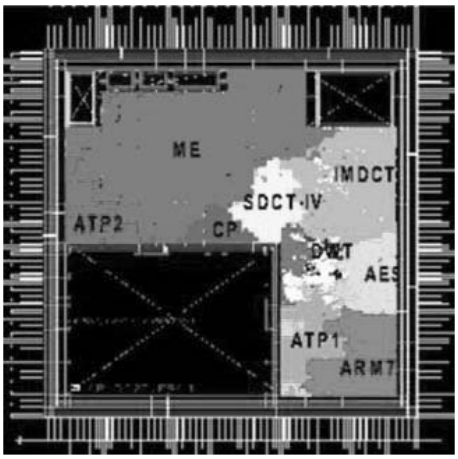
7. BUSINESS OVERVIEW *(Cont'd)*

During the physical design stage, the netlist is converted into a geometric layout, which specifies the placement of components and their interconnections on the silicon die. EDA tools automate routine tasks such as floor planning, placement, clock tree synthesis, power distribution and routing. Despite the automation, our technical personnel actively monitor the process for optimisation and make critical decisions to improve performance, resolve design errors and optimise overall layout.

We use PDKs provided by foundries in all design stages to ensure our IC designs are compatible with the foundries' fabrication parameters and methodologies. PDK contains design rules that define the limitations of the fabrication process and the electrical properties of the fabrication materials. These rules ensure that the design adheres to the fabrication capabilities and meets the required performance standards.

Floor planning

An example of an IC floorplan



Floor planning involves the strategic placement of major function blocks, also known as macros, within the chip's die area. This process considers factors such as macro dimensions, power consumption, performance requirements, I/O placements and routing congestion.

Placement

Placement involves assigning specific locations of individual cells within the floorplan. We use algorithms like simulated annealing, genetic algorithms and analytical placers to optimise wire length, congestion, timing and power.

Clock tree synthesis

Clock tree synthesis involves distributing the clock signal evenly to all sequential elements in the design for proper timing of data transfers throughout the circuit. The goal is to minimise clock skew, which is the difference in arrival time of the clock signal at each sequential element, to meet the timing requirements and contribute to overall system performance.

Power planning and distribution

Power planning and distribution involves designing the power and ground supply network to deliver power efficiently to all circuit components.

Routing

Routing involves connecting the placed components with metal wires to establish the desired circuit functionality, forming a complete layout of an IP. This step is critical for ensuring that the signal integrity and performance requirements are met.

Interposer and package design

Upon customer request, we also perform interposer and package design once the ICs are fabricated by the foundries, to ensure our silicon IP functions optimally at the component level. Key factors in the design process include power delivery, performance requirements such as interconnect and signal integrity, thermal management, size and payout constraints, communication efficiency as well as compatibility with other system components based on the interposer PDK and package design rules provided by several outsourced semiconductor assembly and test service providers.

7. BUSINESS OVERVIEW *(Cont'd)*

Physical verification

The completed physical database will go through extensive verification and testing to ensure the design of the IP meets its specified requirements and adheres to design rules. EDA tools and PDKs are crucial in this process to automate and validate various aspects of the design.

Some of the verification processes are as follows:

- **design rule checking**: to verify the layout adheres to foundry-specific design rules provided in the PDKs, checking parameters such as spacing, width and alignment to prevent fabrication issues;

- **layout versus schematic verification**: ensures the physical layout matches the original schematic, verifying connectivity accuracy and alignment between design intent and physical implementation;

- **timing analysis**: to analyse timing characteristics of the circuit, ensuring the circuit performs within the required parameters;

- **power integrity analysis**: to verify the power distribution network for voltage drops and potential noise issues, ensuring stable power delivery across the layout;

- **signal integrity analysis**: ensures signal quality and stability throughout the circuit to prevent issues such as crosstalk;

These verification steps use EDA tools in conjunction with PDK guidelines to ensure the design is optimised for manufacturability, performance and durability. Once the silicon IP is verified, the design will be included in our IC design libraries.

Tapeout

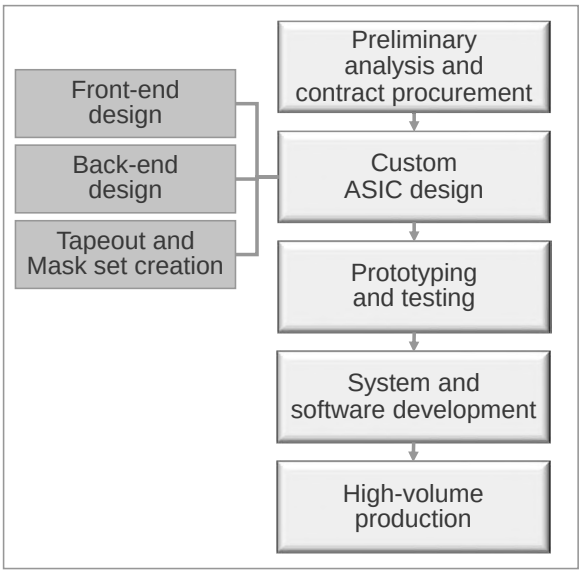
Upon finalisation of the silicon IP design, we create a geometric data file (GDSII) that accurately represents the silicon IP layout for customers to prepare for tapeout. The file is sent to foundries, where the silicon IP is integrated with other silicon IPs to form the full-chip database, followed by creating the mask set and fabricating ICs through the photolithography process.

7.11.2 Design and development of custom ASIC

The design and development of custom ASIC is a complex, multi-stage process that typically takes from several months to a few years, depending on the complexity of the ASIC. The process often involves collaboration among multiple parties, from initial design to high-volume manufacturing.

7. BUSINESS OVERVIEW *(Cont'd)*

Our business process flow for the design and development of custom ASIC for our new customers is depicted below:



Preliminary analysis and contract procurement

Our business operation commenced upon receiving an expression of interest from a prospective customer. Our business development personnel will engage with the customer to understand their needs. We will determine whether to use our existing silicon IPs, develop new silicon IPs, or use third-party IPs to support the functionality of the target product.

Based on the gathered information, we will develop a proposal outlining our solution, project scope, timeline and fee quotation. If our proposal receives initial acceptance, we will fine-tune it after further discussions, resulting in a final statement of work ready for customer acceptance.

Custom ASIC design

Upon securing the contract, our technical personnel team begins the custom ASIC design process. The process includes the front-end and back-end design activities, integrating our silicon IP, third-party IPs and customer's proprietary IPs to create custom ASIC database.

The front-end design process involves architecture and micro-architecture definition, logic design and logic verification to ensure the design meets the required functional specifications. Following this, the back-end design focuses on physical implementation, including floor planning and placement and timing analysis, to ensure the design meets the required performance specifications and to prepare for tapeout. Once the physical verification process is completed, the design is considered final and enters the tapeout phase. The GDSII file from tapeout phase is sent to foundries to create a mask set and fabricate IC through photolithography.

For further details, see Section 7.11.1 of this Prospectus on "design phase", "integration and physical design", "physical verification" and "tapeout".

Prototyping and testing

The mask set is created based on the finalised ASIC design, and the wafer is used to fabricate IC on silicon wafers through photolithography. These wafers are thin and flat silicon slices containing multiple identical copies of the ASIC design. The wafers will be sent to outsourced semiconductor assembly and test service providers to be packaged. Once packaged, the prototypes are ready for system integration, where they are incorporated into the system for further validation and testing.

System and software development

Once the silicon prototypes are being made available, the customer will carry out system and software development focusing on hardware validation, driver development, firmware and system software development and integration, system performance optimisation, and application-level testing. The goal is to ensure the functionality of the prototypes and the target system.

High-volume production

After successful testing, characterisation and qualification, we proceed to high-volume production, which is carried out by foundries and third-party semiconductor assembly and test service providers.

7.12 R&D

We carry out R&D continuously given the evolving technological landscape. As at the LPD, our R&D activities are supported by 318 technical personnel including engineers led by our Chief Technology Officer, Teh Chee Hak. Our R&D activities are also supported by the use of EDA tools and PDKs.

Our R&D activities are focused on the following areas:

- optimise memory access performance, efficiency, and power;
- Network-on-Chip architecture; and
- utilisation of the latest technology.

Through our R&D and product development efforts, we have developed several silicon IPs including DDR, LPDDR and HBM interface IPs. As the original designer, we retain the IP rights to all our designs, enabling us to reuse and adapt them for future applications and resale. We file patents to safeguard our intellectual property and to secure the right to our innovative inventions. As at the LPD, we have 29 patents registered in Malaysia, China and the USA, and 79 patents pending application/registration in Malaysia, China and the USA. See Annexure A of this Prospectus for further details on our patents.

We plan to expand our products and services including our silicon IP portfolio and field of application. We also plan to design and develop new IC products including compute and AI hardware accelerator, and 2.5D/3D silicon products. See Section 7.5 of this Prospectus for further details on our strategies and future plans.

7. BUSINESS OVERVIEW *(Cont'd)*

7.12.1 Optimise memory access performance, efficiency, and power

We carry out R&D to optimise memory access performance, efficiency and power, focusing on the following objectives:

- enhancing the speed of our memory interfaces through advanced techniques such as high-speed design techniques and optimised data paths to improve the performance, efficiency and capability of the IC. Faster memory access enables quicker execution of programs and tasks and reduces latency which is critical for applications requiring real-time processing. High-speed memory interfaces also increase scalability by allowing the system to handle higher workloads without requiring immediate hardware upgrades. This capability facilitates emerging technologies such as fifth-generation mobile communication systems (5G), IoT and autonomous systems that demand rapid data processing and transfer.

- improving power efficiency through implementing advanced design techniques to reduce overall power consumption and enhance system performance. Our LPDDR memory interfaces are developed for low power consumption which is commonly used for mobile and power-critical applications, as well as for the deployment of AI applications.

  As at the LPD, we have successfully designed and commercialised three types of memory interfaces, with the specifications of the latest generations we have commercialised described below:

  - **DDR:** DDR4/5 with maximum data rate per pin of up to 3200 MT/s;
  - **LPDDR:** LPDDR5x with maximum data rate per pin up to 8533 MT/s and above; and
  - **HBM:** HBM3E with a maximum data rate per pin up to 8.0 Gb/s and above.

  In addition, as at the LPD, we are carrying out R&D for LPDDR6 with a maximum rate of up to 14400 MT/s, and HBM4 with a maximum data rate per pin up to 8.0 Gb/s and above. Nevertheless, these memory interface IPs have yet to be commercialised.

7.12.2 Network-on-Chip architecture

We carry out R&D to advance our Network-on-Chip architecture to optimise data flow and memory access patterns to achieve higher data throughput, lower latency, and to improve scalability, reliability and security in multi-core systems.

Key focus areas for optimisation include the following:

- supporting heterogeneous processing to address diverse communication needs across different cores and subsystems;
- enabling reconfigurability and programmability to adapt Network-on-Chip designs to a wide range of applications and workloads; and
- ensuring the architectures are compatible with emerging technologies such as 3D stacking, optical interconnects and quantum computing.

As at the LPD, we offer both coherent and non-coherent Network-on-Chip designs, enabling us to support a wide range of IC products. Our capabilities are further enhanced by the commercialisation of our new generation Network-on-Chip IP in 2024. This new generation includes coherent and non-coherent Network-on-Chip IP with expanded protocol support, improved power efficiency, enhanced performance, and reduced latency and area.

7.12.3 Utilisation of the latest technology

We carry out R&D to utilise the latest technology, focusing on the following objectives:

- Design IC using an advanced process node, facilitated by access to PDKs from foundries to enhance performance, power efficiency and integration density. Our silicon IPs are designed and developed on process nodes down to 4nm.

- Utilise EDA tools for simulation, synthesis and physical design to streamline the design process, which improves accuracy and accelerates the development processes. We also continuously develop in-house design methodology improvements to further streamline the design process.

- Ensure seamless integration of memory interfaces and interconnects within multi-processor systems using our in-house developed integration and configuration software, namely RAPTuner. See Section 7.7.6 of this Prospectus for more information on our in-house developed integration and configuration software.

7.13 TECHNOLOGIES USED

We commonly use the following technologies in our design operations:

- EDA tools;
- PDKs; and
- Verification IPs.

7.13.1 EDA tools

EDA tools refer to software applications used in IC design processes. These tools automate various aspects of the design functions, thereby increasing efficiency and improving accuracy.

The common types of EDA tools that we use in our design operation are as follows:

- **Design entry tools**, which take a proposed circuit function and assemble the elements needed to build it, providing both physical and logical directions. They help create the appropriate geometric shapes and provide insight into how to connect these integral components.

- **Simulation tools** such as those used for prototyping, predict a circuit's behaviour by modelling its performance in the real world. This eliminates the need for trial and error by allowing design engineers to foresee how the circuit will operate under various conditions.

- **Verification tools** are used to ensure that an IC or chip meets expectations and performs the desired behaviours. These tools ensure compliance with design specifications and compare the actual function of the circuit to its predicted function. They also confirm that the interconnected parts of a circuit work together harmoniously.

7.13.2 PDK

PDK refers to a comprehensive collection of data used in the design of IC. PDK is typically provided by foundries and contains all the necessary information to ensure that an IC design is compatible with a specific manufacturing process. They include essential information, tools and guidelines that ensure manufacturability, enhance design accuracy, streamline the design process and maintain consistency across different components of the IC.

7. BUSINESS OVERVIEW *(Cont'd)*

The key components of a PDK are as follows:

- **Design rules** are guidelines that define the physical constraints for layout design, such as minimum feature sizes, spacing between components and layer-specific rules. These ensure that the design can be reliably manufactured.

- **Design rule checking files**, which are files and scripts used to verify the layout adheres to the design rules to ensure design correctness and manufacturability.

- **Process parameters**, which are detailed information about the semiconductor fabrication process, including material properties and interconnect layer thicknesses. These are to accurately model the behaviour of the IC during simulation.

- **Standard cell libraries**, which are predefined logic gates of standard components such as NAND, NOR and XOR that can be easily resized and utilised by EDA tools for physical placement and routing.

- **Models**, which are electrical models of the components, including resistance, capacitance and inductance parameters are important for accurate circuit simulation and signal integrity analysis.

7.13.3 Verification IPs

Verification IPs are pre-designed independent verification models to validate the compliance of the IC design to industry standards and protocols. They are pre-built, reusable components used to simulate, monitor and test the behaviour of interfaces and protocols during the design verification process. Some industry standards that we follow include JEDEC and UCIe. Verification IPs are used in conjunction with EDA tools.

7.14 SEASONALITY

During the Financial Years Under Review and up to the LPD, we did not experience any material seasonality in our business.

7.15 MATERIAL INTERRUPTIONS IN OUR BUSINESS

We did not experience any material interruptions to our business operations during the past 12 months of our operations before the LPD. Additionally, as we can work remotely, we did not experience any material interruptions to our business operations due to the effects of COVID-19 during the Financial Years Under Review and up to the LPD.

7.16 SALES AND MARKETING ACTIVITIES

Our sales and marketing activities and strategies are targeted towards the following:

- We are positioned as an IC design company specialising in silicon IP and silicon products. As at the LPD, we are supported by 318 technical personnel including engineers in various disciplines including electrical and electronic, computer and software engineering. We market our technical expertise in multi-interface protocol architecture for high-speed interconnect and memory interface systems. Our skill set spans digital, analogue and mixed-signal designs, design-for-test, physical design, custom layout, packaging design, and silicon characterisation and verification.

7. BUSINESS OVERVIEW *(Cont'd)*

- We also position ourselves as an original designer of various types of silicon IPs, we hold the rights to our designs supported by patents in Malaysia and foreign countries. As at the LPD, we have 29 patents registered in Malaysia, China and the USA, and 79 patents pending application/registration in Malaysia, China and the USA.

- In general, our business development team adopts a systematic approach to secure new customers. Some of the key steps are as follows:

  - **Initial engagement**: We adopt an active business development approach by continuously engaging with potential customers to understand their requirements. We will provide solutions that address their needs by leveraging market and technology trends, as well as our engagement in industry standards. We are involved in the review and recommendation of JEDEC standards through the involvement of our Chief Technology Officer, Teh Chee Hak. Our involvement increases our profile in the industry which helps us in our sales and marketing activities. More importantly we are aware of impending new standards arising from our involvement with reviewing and recommending JEDEC standards.

    We engage with potential target customers by participating in industry conferences and events, showcasing our capabilities in technological advancements and new IP offerings. In addition, we present at these events to showcase our capabilities and establish networks and foster connections with peers and potential customers.

  - **Engaging in technical discussion**: We conduct technical discussions with potential customers to understand their technical requirements and present product features demonstrating our technological capabilities.

  - **Providing tools for customer evaluation**: Following the technical discussion, we offer evaluation kits which are demonstration tools or simulation models that we developed for customer evaluation. This allows potential customers to test our silicon IPs in their operational and development environment.

  - **Follow-up and negotiation**: We follow up on the feedback gathered from the evaluation tools to address their needs and concerns, and this will be used to refine our offerings for the preparation of a proposal. Our proposal will outline terms, pricing and any additional services offered and there will be further discussion to finalise the contract ensuring that all terms are aligned between both parties.

  - **Closing the deal**: The contract will be formalised upon the signing of the contract. Our technical team will then commence the onboarding process for the project based on the contract signed.

  - **Post-sales and development phase support**: Our business development team will continue to maintain regular communication to provide support and updates to ensure customer satisfaction. At the same, our technical team will also actively provide support during the development phase and silicon bring-up phase to ensure customers receive guidance and technical resources throughout both the development phase and silicon bring-up phase to ensure smooth integration. In addition, we also involve collaboration with EDA tool providers and foundries during the development phase.

7. BUSINESS OVERVIEW *(Cont'd)*

- For the Financial Years Under Review and up to the LPD, industry events and conferences that we have attended include:

Year	Description	Location
May 2023	COMPUTEX Taiwan 2023	Taiwan
January 2024	Consumer Electronic Show (CES) 2024	USA
April 2024	KL20 Summit 2024	Kuala Lumpur
June 2024	27th TSMC Technology Symposium Japan	Yokohama Bay Hotel Tokyu, Japan
August 2024	Synopsys Users Group (SNUG) Penang 2024	Malaysia
September 2024	TSMC North America 2024 Open Innovation Platform Ecosystem Forum	USA
March 2025	Launching Ceremony Strategic Partnership in The Semiconductor Industry	Malaysia
July 2025	CadenceCONNECT Southeast Asia – Malaysia Technology Seminar 2025	Malaysia

- In view of the requirements for specialised technical knowledge required to promote silicon IP and custom ASIC designs, our sales and marketing team is led by our Chief Executive Officer, Dato' Fong Swee Kiang who has over 35 years of experience in the semiconductor industry. As at the LPD, we have 3 business development personnel in Malaysia. Our business development team works alongside our technical personnel team led by our Chief Technology Officer, Teh Chee Hak.

- In addition, as at the LPD, we have appointed 2 sales representatives in China, and appointed a sales representative in the USA to source sales leads to help grow our business.

7.17 MAJOR CUSTOMERS

Our top 5 major customers by revenue for the Financial Years Under Review are as follows:

FYE 31 March 2023

Name	Country of origin	Main type of products and services	RM'000	% of our revenue	Length of relationship[(1)] (year(s))
Customer A[(2)]	China	Custom silicon IP	33,236	58.1	3
Customer B[(4)]	Taiwan	Network-on-Chip IP	18,004	31.5	Less than 1
IC Works[(3)]	Malaysia	Memory interface IP	3,984	7.0	2
Customer C[(5)]	China	Memory interface IP	1,935	3.4	Less than 1
Sub-total			**57,159**	**100.0**	
Group Revenue			**57,159**		

7. BUSINESS OVERVIEW *(Cont'd)*

FYE 31 March 2024

Name	Country of origin	Main type of products and services	RM'000	% of our revenue	Length of relationship[(1)] (year(s))
Customer B[(4)]	Taiwan	Network-on-Chip IP	19,136	24.8	1
Customer A[(2)]	China	Custom silicon IP	18,897	24.5	4
Customer D[(6)]	China	Memory interface IP	15,611	20.3	1
Customer E[(7)]	China	Custom silicon IP	9,315	12.1	1
Customer F[(8)]	China	Memory interface IP	4,766	6.2	Less than 1
Sub-total			**67,725**	**87.9**	
Group Revenue			**77,063**		

FYE 31 March 2025

Name	Country of origin	Main type of products and services	RM'000	% of our revenue	Length of relationship[(1)] (year(s))
Customer D[(6)]	China	Custom ASIC, memory interface and Network-on-Chip IP	32,229	27.0	2
Customer G[(9)]	Taiwan	Custom ASIC	27,931	23.4	1
Customer B[(4)]	Taiwan	Network-on-Chip IP	12,066	10.1	2
Customer H[(10)]	Malaysia	Memory interface IP	9,704	8.1	Less than 1
Customer I[(11)]	China	Memory interface IP	8,454	7.1	1
Sub-total			**90,384**	**75.7**	
Group Revenue			**119,503**		

Notes:

(1) Length of relationship as at the end of the respective financial year, where the numbers are rounded up to the nearest whole year if it is 6 months or more and vice versa.

(2) Customer A is a private company located in China which involved in research and development, and sales of programmable system platform chips and software tools. The name of Customer A has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(3) A related party company involved in research and development on engineering and technology, management consultancy activities as well as business support service activities, and is in the midst of winding up. See Section 10.1 of this Prospectus for further details.

7. BUSINESS OVERVIEW *(Cont'd)*

(4) Customer B is fabless semiconductor company listed on the Taiwan Stock Exchange, which is involved in design and development of ICs for mobile device, home entertainment, connectivity and IoT products. The name of Customer B has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(5) Customer C is a private company in China and provides interface IPs and chiplet solutions. The name of Customer C has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(6) Customer D is a private company in China, which is involved in software development and IC design, chip and product manufacturing and others. The name of Customer D has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(7) Customer E is a private company in China which is involved in design, development and sales of IC. Customer E is a subsidiary of a company listed on the Taiwan Stock Exchange. The name of Customer E has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(8) Customer F is a private company in China, which is involved in chip design. Customer F is related to a company listed on the NASDAQ in the USA and Hong Kong Stock Exchange in Hong Kong. The name of Customer F has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(9) Customer G is a private company in Taiwan which is involved in design and development of ASIC. The name of Customer G has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(10) Customer H is a private company in Malaysia which is involved in R&D of engineering and technology, wholesale of computer hardware, software and peripherals, as well as manufacture of computers. The name of Customer H has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

(11) Customer I is a private company in China which is involved in various activities including IC design, chip and product manufacturing. The name of Customer H has not been disclosed as our Group is unable to obtain consent, and the information is commercially sensitive.

We are not dependent on certain customers as our business is project-based and our contract period ranges from 1 to 3 years for sales of silicon IP. The nature of project-based business allows us to continually secure additional contracts from existing customers or contracts from new customers. For the Financial Years Under Review, our customer base increased from 4 customers for the FYE 31 March 2023 to 14 customers for the FYE 31 March 2025.

Furthermore, revenue contributions from our customers are based on milestones stipulated in the contracts. In this respect, the revenue contribution of certain customers may decrease as the work is nearing completion and approaching the end of the contract.

7. BUSINESS OVERVIEW *(Cont'd)*

7.18 TYPES AND SOURCES OF INPUT SERVICES

The costs incurred for purchases of input products and services for the Financial Years Under Review are set out below:

	FYE 31 March					
	2023		2024		2025	
	RM'000	%	RM'000	%	RM'000	%
Software tools	1,046	46.3	3,145	85.7	4,776	46.2
Semiconductor materials and manufacturing services	-	-	-	-	3,078	29.7
Outsourcing of IC and printed circuit board design and assembly services	1,211	53.7	524	14.3	2,281	22.0
Product sales support to promote silicon IP licensing	-	-	-	-	214	2.1
Total operational costs (1)	**2,257**	**100.0**	**3,669**	**100.0**	**10,349**	**100.0**

Note:

(1) Total operational costs refer to products and services purchased from third-party suppliers and/or service vendors, which comprise software tools and related expenses incurred, purchase of semiconductor materials and manufacturing services, outsourcing of IC and printed circuit board design and assembly services as well as product sales support to promote silicon IP licensing.

For the Financial Years Under Review, the main products and services rendered by suppliers and/or service vendors comprise the following:

- Software tools where we license the use of software tools from various providers including Synopsys (through the sole distributor in Malaysia for Synopsys), Ansys, and Siemens. These are used for our design and development operations.

- Purchase of semiconductor materials and manufacturing services for the production of our custom ASIC products.

- Costs for outsourcing of IC and printed circuit board design and assembly services where we engaged third parties to perform design and assembly services, including circuit design and custom layout, for us based on our specifications. The services are based on an ad-hoc basis when it is required.

- Product sales support to promote silicon IP licensing where we engaged third-party company to provide sales support services to promote the sales/licensing of our silicon IP in China as stipulated in the agreement.

7.19 MAJOR SUPPLIERS

Our top 5 major suppliers by operational costs incurred for the Financial Years Under Review are as follows*:

FYE 31 March 2023

Name	Country (based on billing)	Main type of products and/or services	RM'000	% of our total operational costs	% of our cost of sales	Length of relationship(1) (year(s))
Alten	India	Outsourcing of IC design services	1,121	49.6	4.8	2
ICE	Malaysia	Subscription of EDA tools and/or Verification IP	1,046	46.4	4.5	3
Ansys	USA					2
Tessolve Semiconductor Pvt Ltd ("**Tessolve**")	India	Outsourcing of IC design services	51	2.3	0.2	Less than 1
Mnosys Sdn Bhd ("**Mnosys**")	Malaysia	Outsourcing of printed circuit board design services	30	1.3	0.1	Less than 1
Sub-total			**2,248**	**99.6**	**9.6**	
Total operational costs(2)			**2,257**			
Total cost of sales(3)			**23,371**			

7. BUSINESS OVERVIEW *(Cont'd)*

FYE 31 March 2024

Name	Country (based on billing)	Main type of products and/or services	RM'000	% of our total operational costs	% of our cost of sales	Length of relationship[1] (year(s))
ICE	Malaysia	Subscription of EDA tools and/or Verification IP	3,215	87.6	7.8	4
Ansys	USA					3
Siemens Electronic Design Automation Pte Ltd ("**Siemens**")	Singapore					Less than 1
Tessolve	India	Outsourcing of IC design services	134	3.7	0.3	1
Mnosys	Malaysia	Outsourcing of printed circuit board assembly services	38	1.0	0.1	1
Sub-total			**3,387**	**92.3**	**8.2**	
Total operational costs[2]			**3,669**			
Total cost of sales[3]			**41,034**			

7. BUSINESS OVERVIEW *(Cont'd)*

FYE 31 March 2025

Name	Country (based on billing)	Main type of products and/or services	RM'000	% of our total operational costs	% of our cost of sales	Length of relationship[1] (year(s))
ICE	Malaysia	Subscription of EDA tools and/or Verification IP	4,785	46.3	7.0	5
Ansys	USA					4
Siemens	Singapore					1
Supplier A[4]	USA	Purchase of semiconductor materials and manufacturing services	3,047	29.4	4.4	2
Shanghai Lomicro Information Technology Co Ltd	China	Product sales support to promote silicon IP licensing	214	2.1	0.3	1
Sub-total			**8,046**	**77.8**	**11.7**	
Total operational costs[2]			**10,349**			
Total cost of sales[3]			**69,058**			

Notes:

* *The grouping of the operational costs of our Group's EDA Tools and Verification IP Suppliers is due to strategic business and competitive reasons, aimed at safeguarding our Group's negotiating position and supplier relationships.*

(1) Length of relationship as at the end of the respective financial year, where the numbers are rounded up to the nearest whole year if it is 6 months or more and vice versa.

(2) Total operational costs comprise products and services purchased from third-party suppliers and/or service vendors, which comprise software tools and related expenses incurred, purchase of semiconductor materials and manufacturing services, outsourcing of IC and printed circuit board design and assembly services as well as product sales support to promote silicon IP licensing.

(3) Total cost of sales comprises total operational costs, technical staff costs, lab rental and depreciation of prototype equipment and engineering tools.

7. BUSINESS OVERVIEW *(Cont'd)*

(4) Supplier A is a company incorporated in the USA, mainly involved in the sales and marketing of ICs and semiconductor devices. Supplier A is a subsidiary of a semiconductor foundry that is listed on the Taiwan Stock Exchange and the New York Stock Exchange with headquarters in Taiwan, and the company is mainly involved in the manufacturing, sales, packaging, testing and computer-aided design of ICs and other semiconductor devices, and the manufacturing of masks. The name of Supplier A has not been disclosed as our Group is unable to obtain consent, and the disclosure of such information may lead to possible adverse business implications with Supplier A, for which our Group is committed to safeguarding this key collaboration.

7. BUSINESS OVERVIEW *(Cont'd)*

We are dependent on the EDA Tools and Verification IP Suppliers as the software tools and IPs are essential to our IC design process. These EDA tools and Verification IP are highly specialised and there are only a limited number of viable alternative suppliers which can fulfil our Group's requirements.

Since 2020, we have been utilising a comprehensive suite of core EDA tools purchased from Synopsys, either directly or through ICE (which is the sole distributor in Malaysia for Synopsys). These tools, categorised as standard EDA tools, are essential for key aspects of IC design, such as logic, circuit and physical design. In our view, there is only one viable alternative provider, namely Cadence, which offers a comparable suite of EDA tools that supports the entire IC design flow which can fulfil our Group's requirements. As at the LPD, we have started purchasing EDA tools from Cadence. We also utilise specialised EDA tools from Siemens for IC verification and design for manufacturability optimisation.

To address specialised design needs, we use tools from Ansys in IC package design, which includes signal integrity, power delivery and reliability simulations. These tools are critical for optimising the performance and durability of IC packages, and there is only a limited number of alternative suppliers for these specialised tools which can fulfil our Group's requirements. In July 2025, Ansys became part of the Synopsys group of companies.

We also source Verification IP from Synopsys (through ICE) and Siemens, for which there is only a limited number of alternative suppliers which can fulfil our Group's requirements. Verification IP ensures compliance with industry standards and supports interoperability across a wide range of applications.

Compatibility between semiconductor foundry processes and EDA tools often determines the choice of tools. As such, our Group's reliance on the EDA Tools and Verification IP Suppliers is driven by technical compatibility and business needs. This reliance evolves dynamically with changing design requirements and advancements in foundry technologies. By leveraging a balanced mix of core and specialised EDA tools, we will be able to maintain operational flexibility and our competitive edge in the IC design industry.

In addition, we are also dependent on a semiconductor foundry for the manufacturing and delivery of our prototypes and custom ASIC products.

7.20 EMPLOYEES

As at the LPD, we employ a total of 338 employees, all of whom are permanent employees. The breakdown of our employees by department is as follows:

Designation / Department	As at the LPD
Executive Directors and Key Senior Management	6
Engineering	318
Business Development	3
Accounts and Finance / Administrative / Human Resources	7
Information Technology	4
Total	**338**

Note:

As at the LPD, we have a total of 9 independent contractors.

As at the LPD, the breakdown of our employees by country is as follows:

	As at LPD		
Country	**Local**	**Foreign**	**Total**
Malaysia	315	4	**319**
Vietnam	19	-	**19**
Total	**334**	**4**	**338**

All of our foreign employees possess valid working permits and/or documentations. Our foreign employees are primarily employed as our engineers. As at the LPD, none of our employees belong to any trade union.

During the Financial Years Under Review and up to the LPD, there was no major industrial dispute involving our employees. During the same period, we did not face any labour shortage that led to any disruption to our business operations.

7.21 INSURANCE

We maintain employee benefits insurance for our employees. The insurance policy that we currently hold is customary in the industry in which we operate, and we will review our insurance coverage annually.

7.22 MATERIAL DEPENDENCY ON COMMERCIAL CONTRACTS, AGREEMENTS AND OTHER ARRANGEMENTS

As at the LPD, there are no commercial contracts, agreements, other arrangements or other matters entered into by or issued to us which we are materially dependent on, and which are material to our business and profitability.

7.23 PATENTS, TRADEMARKS AND OTHER INTELLECTUAL PROPERTY RIGHTS

Details of our patents and trademarks are set out in Annexure A of this Prospectus.

7.24 GOVERNING LAWS AND REGULATIONS RELATING TO OUR INDUSTRY

The relevant laws and regulations governing our Group and which are material to our operations are summarised below. The following does not purport to be an exhaustive description of all relevant laws and regulations which our business is subject to.

(i) Local Government Act 1976 ("LGA 1976")

The LGA 1976 is enacted to revise and consolidate the laws relating to local government in Peninsular Malaysia. Pursuant to Section 107(2) of the LGA 1976, every licence or permit granted by the local authority shall be subject to such conditions and restrictions as the local authority may think fit and shall be revocable by the local authority at any time without assigning any reason therefor.

Pursuant to Section 107(6) of the LGA 1976, a person who fails to exhibit or produce his licence on the licensed premises shall be guilty of an offence and shall on conviction be liable to a fine not exceeding RM500.00 or to imprisonment for a term not exceeding 6 months or to both such fine and imprisonment.

(ii) Employment Act 1955 ("EA 1955")

The EA 1955 regulates all labour related matters including contracts of service, payment of wages, pregnancy and maternity protection, rest days, hours of work, holidays, termination, lay-off and retirement benefits, employment of foreign employees and keeping of registers of employees.

Any person who commits any offence under, or contravenes any provision of the EA 1955, or any regulations, order or other subsidiary legislation whatsoever made thereunder, in respect of which no penalty is provided, shall be liable, on conviction, to a fine not exceeding RM50,000.00.

(iii) Patents Act 1983 ("PA 1983") and Patents Regulations 1986 ("PR 1986")

The PA 1983 and PR 1986 are the laws and regulations which govern patent protection in Malaysia. The PA 1983 would cover, among others, the criteria for patentability, rights attached to patents, duration of patents and acts relating to infringement, whereas the PR 1986 predominantly encompass the procedures for the application of patents.

Pursuant to Section 11 of the PA 1983, an invention is patentable if it is new, involves an inventive step and is industrially applicable. Section 12 of the PA 1983 provides that an invention which may relate to a product or process means an idea of an inventor which permits in practice the solution to a specific problem in the field of technology. Section 36 of the PA 1983 provides that the registration of a patent grants the patent owner exclusive rights to exploit the patented invention, to assign or transmit the patent, to conclude licence contacts and to deal with the patent as the subject of a security interest.

Pursuant to Section 31 of the PA 1983, a patent shall be deemed granted on the date the certificate of grant of patent is issued. Section 35 of the PA 1983 provides that the duration of a patent will generally be for a period of 20 years from the filing date of the application.

7.25 NON-COMPLIANCES WITH THE RELEVANT LAWS, REGULATIONS, RULES AND REQUIREMENTS GOVERNING THE CONDUCT OF THE OPERATIONS OF OUR GROUP

As at the LPD, there are no breaches of laws, regulations, rules and requirements governing the conduct of the operations of our Group which may have a material adverse impact on our Group's operations.

7.26 MAJOR LICENCES, PERMITS AND APPROVALS

We have various licences and permits for our operations in Malaysia and other jurisdictions where we operate. The details of our major licences, permits and approvals for our operations as at the LPD are as follows:

Malaysia

No.	Licensee	Approving Authority	Description of Licence / Permit	Licence No. / Reference No. / Registration No.	Validity Period	Salient Conditions	Status of Compliance
1.	SkyeChip	Majlis Bandaraya Pulau Pinang	Business premise licence for the premise located at 1-18-12, Suntech @ Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Lepas, Pulau Pinang.	KOM00010347	19 November 2024 to 31 December 2025	Nil	Complied
2.	SkyeChip	Majlis Bandaraya Pulau Pinang	Business premise licence for the premise located at 1-17-1, Suntech @ Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Lepas, Pulau Pinang.	KOM00014666	15 November 2024 to 31 December 2025	Nil	Complied
3.	SkyeChip	Majlis Bandaraya Pulau Pinang	Business premise licence for the premise located at 1-17-02, Suntech @ Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Lepas, Pulau Pinang.	KOM00014745	22 November 2024 to 31 December 2025	Nil	Complied
4.	SkyeChip	Majlis Bandaraya Pulau Pinang	Business premise licence for the premise located at 1-20-01, Suntech @ Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Lepas, Pulau Pinang.	KOM00014793	3 December 2024 to 31 December 2025	Nil	Complied

7. BUSINESS OVERVIEW (*Cont'd)*

Vietnam

No.	Licensee	Approving Authority	Description of Licence / Permit	Licence No. / Reference No. / Registration No.	Validity Period	Salient Conditions	Status of Compliance
1.	SkyeChip Da Nang	Department of Science and Technology of Da Nang City	Confirmation on SkyeChip Da Nang's engagement in semiconductor activities for the purposes of tax incentives eligible under the laws of Vietnam	1772/SKHCN-HTS	Nil	Nil	Complied
2.	SkyeChip Da Nang	Department of Finance of Da Nang City	Investment registration certificate as an approval for a foreign investor to invest in Vietnam as well as a license in favour of SkyeChip Da Nang to implement the investment project for the establishment of SkyeChip Da Nang in Vietnam	1017385161	2 January 2025 to 1 January 2035	Nil	Complied
3.	SkyeChip Da Nang	Department of Finance of Da Nang City	Enterprise registration certificate as a document recording the incorporation and corporate information of SkyeChip Da Nang as a company incorporated in Vietnam	0402261114	Nil	Nil	Complied
4.	SkyeChip HCMC	Department of Finance of Ho Chi Minh City	Investment registration certificate as an approval for a foreign investor to invest in Vietnam as well as a license in favour of SkyeChip HCMC to implement the investment project for the establishment of SkyeChip HCMC in Vietnam	9800380408	10 January 2025 to 9 January 2075	Nil	Complied
5.	SkyeChip HCMC	Department of Finance of Ho Chi Minh City	Enterprise registration certificate as a document recording the incorporation and corporate information of SkyeChip HCMC as a company incorporated in Vietnam	0318827592	Nil	Nil	Complied

7.27 MATERIAL PROPERTIES AND EQUIPMENT

7.27.1 MATERIAL PROPERTY OWNED BY OUR GROUP

As at the LPD, we do not own any material property.

7.27.2 MATERIAL PROPERTIES LEASED / RENTED BY OUR GROUP

As at the LPD, the details of the material properties leased / rented by our Group are as follows:

Malaysia

No.	Name of lessor/lessee or landlord/tenant or tenant or sub-tenant/ Postal address	Description of property/ Existing use	Date of issuance of CCC or equivalent	Built-up area (square metres unless otherwise stated)	Period of tenancy or lease	Monthly rental (RM unless otherwise stated)
1.	Emerald Capital Development Sdn Bhd(1) (landlord) / SkyeChip (tenant) 1-17-01, Suntech @ Penang Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Baru, Pulau Pinang	An office unit at 17th floor of a 23-storey commercial / office complex / Office	20 June 2008	792	Until 15 August 2026 or the completion of the disposal of the property by the landlord, whichever earlier(1)	30,000.00
2.	Suiwah Holdings Sdn Bhd (landlord) / SkyeChip (tenant) 1-17-02, Suntech @ Penang Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Baru, Pulau Pinang	An office unit at 17th floor of a 23-storey commercial / office complex / Office	20 June 2008	6,867 sq ft	3 years up to 30 September 2027	21,630.00
3.	Foong Siew Yee and Teh Beng Swan (landlords) / SkyeChip (tenant) 1-18-12, Suntech @ Penang Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Baru, Pulau Pinang	An office unit at 18th floor of a 23-storey commercial / office complex / Office	20 June 2008	608	3 years up to 14 October 2026 (with an option to renew for a further 3 years)	22,800.00

7. BUSINESS OVERVIEW (*Cont'd)*

No.	Name of lessor/lessee or landlord/tenant or tenant or sub-tenant/ Postal address	Description of property/ Existing use	Date of issuance of CCC or equivalent	Built-up area (square metres unless otherwise stated)	Period of tenancy or lease	Monthly rental (RM unless otherwise stated)
4.	Suiwah Holdings Sdn Bhd (landlord) / SkyeChip (tenant) 1-20-01, Suntech @ Penang Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Baru, Pulau Pinang	An office unit at 20th floor of a 23-storey commercial / office complex / Office	20 June 2008	1,902	3 years up to 31 August 2028 (with an option to renew for a further 3 years)	67,151.44
5.	SIDEC (sub-lessor) / SkyeChip Semi (sub-lessee) Lot No. 3F-1&2, 3rd Floor, Tower 4 @PFCC, Jalan Puteri 1/2, Bandar Puteri, 47100 Puchong, Selangor	An office unit at 3rd floor of a 21-storey commercial office / Office	1 December 2014	7,660 sq ft	3 years up to 31 March 2028	22,978.50(2)

Notes:

(1) Persons connected to our Promoters have agreed to acquire Unit No. 1-17-01, Suntech @ Penang Cybercity, Lintang Mayang Pasir 3, 11950 Bayan Baru, Pulau Pinang. Our Company intends to continue the tenancy in relation to this premise upon completion of the sale of the property.

(2) SkyeChip Semi was granted a monthly rental subsidy capped at RM827,226.00 for the term of the tenancy.

7.27.3 MATERIAL PLANT, MACHINERY AND EQUIPMENT

As at the LPD, the material plant and equipment owned by our Group comprise prototypes for HBM interface IP and engineering tools which are mask sets for IoT ASIC.

The details of the material plant, machinery and equipment owned by our Group are as follows:

No.	Description / Existing use	Audited NBV as at 31 March 2025 (RM)
1.	Prototypes for HBM interface IP	3,953,837
2.	Engineering tools which are mask sets for IoT ASIC	27,394,534

7.28 ENVIRONMENTAL, SOCIAL AND GOVERNANCE PRACTICES

We are dedicated to achieving excellence in sustainability within our business by operating with environmental and social responsibility and upholding high standards of corporate governance. Our Group's ESG practices include the following:

7.28.1 Environmental

We acknowledge the importance of safeguarding the environment and are dedicated in integrating several environmentally sustainable principles and practices into our operations by focusing on the following areas:

(i) Energy Efficiency

We are in the early stages of our energy conservation efforts and are diligently monitoring our energy consumption while implementing energy-saving measures. One key initiative is the extensive use of energy-efficient light-emitting diodes ("**LED**") across our operations. LEDs consume significantly lesser energy than traditional light bulbs, have a longer lifespan and produce less heat, all of which help to reduce energy usage. The utilisation of LED lighting demonstrates our commitment in reducing energy consumption and lowering our carbon footprint.

To complement these initiatives, we have also established simple yet effective house rules to encourage responsible energy use in our workplace. Air conditioning ("**AC**") systems are programmed to operate on an automatic schedule to optimise usage, and all employees are encouraged to switch off lights when leaving a room. These collective efforts help to further conserve energy and embed sustainability into our day-to-day operations.

In addition, we are actively exploring new energy effiency initiatives to further minimise the environmental footprint of our operations while promoting resource efficiency and sustainability.

(ii) Emission Management

In line with Malaysia's nationally determined contributions' target of reducing carbon emission intensity against its gross domestic product by 45% by 2030 as compared to 2005 levels and the global aspiration of achieving net-zero economy's greenhouse gasses ("**GHG**") emissions by 2050, we recognise the importance of aligning our future strategies with these goals.

While our Group does not currently have specific GHG reduction targets or initiatives or reduction plans in place, we remain committed to contributing meaningfully within the context of our operations. As a non-manufacturing company, our GHG emissions primarily stem from electricity consumption in our office premises. In this regard, we encourage sustainable commuting practices among employees by encouraging carpooling, public transportation usage and hybrid work arrangements to reduce travel-related emissions.

(iii) Water Management

We are committed to responsible water management practices as part of our sustainability efforts. Although our water consumption is limited to essential uses such as drinking water and sanitary facilities, we encourage employees to adopt water-saving habits in the workplace. Routine maintenance and checks are conducted to promptly identify and address any potential leakage, ensuring minimal wastage.

7.28.2 Social

Our commitment to social responsibility encompasses active community engagement, diversity and inclusion, health and safety initiatives, and training and education. Some of the key components that are integral to our business philosophy include the following:

(i) Diversity and inclusion

We value diversity and fairness by ensuring our workplace fosters an environment where all employees are valued and have equal opportunities for growth. Our human resource policies are aligned with the national labour laws, namely the Employment Act 1955, Malaysian Anti-Corruption Commission Act 2009 and Personal Data Protection Act 2010.

As at the LPD, our workforce comprises 99% local employees and 1% foreign employees, with 74% male and 26% female representation. Our Group is committed to recruitment, development and advancement practices that are solely based on an individual's qualifications, performance, skills and experience. This ensures that every employee, regardless of background, has equal opportunities to thrive and succeed within our organisation.

(ii) Discrimination and harassment

We strictly prohibit discrimination, harassment, abusive conduct and bullying, which is in accordance with the guidelines outlined in our employee handbook. We are dedicated to fostering a workplace where all employees can work in a safe and respectful environment. As at the LPD, there were no recorded cases of discrimination or harassment within our Group.

(iii) Training and education

We acknowledge the importance of continuous learning and development. To this, we have established several training initiatives aimed to enhance the knowledge and skills of our employees. Our Group's training programs are designed to equip employees with advanced knowledge and practical skills in IC design, verification and optimisation. These courses focus on digital and analog very large-scale integration ("**VLSI**") design, low-power systems, hardware modeling and scripting techniques, equipping employees with the expertise required for designing IPs and ICs for high-performance computing and AI applications. We also provide structured training programs for newly recruited engineers, emphasising advanced IC design and verification across both digital and analog VLSI methodologies. Each engineer is required to complete 110 hours of training, consisting of 25 modules within their first year of employment. This training aims to further enhance our employees' technical knowledge and skillsets.

(iv) Occupational health and safety

At the heart of our efforts is our Group's Health and Safety Policy, with the primary aim of providing a safe and healthy workplace. The chairman of our Health, Safety and Environment ("**HSE**") committee oversees safety across all our Group's operations and we conduct regular reviews and assessments to foster continuous improvement. These assessments cover various safety aspects, including ensuring emergency doors and evacuation plans are properly set up and are functional, first aid boxes are easily accessible with unexpired medications, emergency contact numbers are clearly printed and accessible, pathways remain unobstructed, fire extinguishers are within their respective validity periods and exit signs are illuminated, unblocked and operable under all conditions. Our HSE committee provides checklists and establishes guidelines for incident investigation and prevention, and conducts quarterly meetings to review our Group's safety policies and procedures. Additionally, our Group conducts annual fire drill exercises to enhance emergency preparedness in case of emergencies.

As at the LPD, there were no recorded cases of work-related fatalities, injuries or fines by regulatory authorities for non-compliances in relation to HSE within our workplace.

(v) Local communities

We view community investment as a way to enhance employee engagement, strengthen industry relationships and build a positive corporate reputation. During the period from 1 April 2023 up to the LPD, we sponsored several final-year projects in relation to IC design for students at prominent universities, including Universiti Teknologi Malaysia, Universiti Putra Malaysia and Universiti Malaysia Perlis which amounted to RM280,013. These sponsorships were aimed to foster innovation among future professionals.

In addition to our academic sponsorships, we value the importance of our employees' well-being and cultural inclusivity. We aim to cultivate a vibrant workplace culture that reflects our commitment to fostering a sense of community and inclusivity within our Group.

7.28.3 Governance

We are committed to achieving and sustaining a high standard of corporate governance. We believe that strong and effective corporate governance helps to cultivate a company culture of integrity. To achieve this goal, we have adopted the recommendations of the MCCG, focusing on enhancing board leadership and effectiveness, strengthening audit and risk management practices, ensuring integrity in corporate reporting and fostering meaningful engagement with our stakeholders. As at the LPD, 2 out of 6 members of our Board are women, which is in line with the MCCG's recommendation to have at least 30% women directors.

To ensure strong governance and effective practices, we have implemented the following policies:

- Anti-bribery and corruption policies and procedures - This policy ensures compliance with the Malaysian Anti-Corruption Act 2009. We have also established fundamental standards and a framework aimed at preventing and detecting bribery and corruption within our Group's operations;

- Code of conduct and ethics - This policy ensures clear ethical standards, guiding behaviour, fosters accountability and contributes to a culture of integrity within our Group;

- Whistleblowing policy - This policy ensures adherence to the Whistleblower Protection Act 2010 and allows stakeholders to report any credible suspicious or allegations of fraud, unethical behavior or improper business practices within our Group;

- Data loss prevention policy - This policy safeguards sensitive data from unauthorised access, use and disclosure, fostering a culture of data security and ensuring compliance with regulatory requirements to protect our Group's operational integrity;

- Data disaster recovery policy - This policy establishes a structured approach to ensure business continuity during a disaster, outlining detailed procedures, roles and objectives for effective data recovery and restoration within our Group;

- Related party transaction policy - This policy ensures that all related party transactions and recurring related party transactions in the ordinary course of business are undertaken at arm's length and on normal commercial terms. These transactions should not confer undue benefits to related parties compared to terms generally available to third parties and must not prejudice the interests of non-interested shareholders; and

- Fit and proper policy - This policy is intended to set out the fit and proper criteria for the appointment and re-appointment of directors of our Group and to ensure that each director of our Group has integrity, experience, competence and time in order to discharge his/her role as a director of our Group effectively.

These policies and practices collectively ensure that our operations are conducted in accordance with ethical, regulatory and professional standards, fostering clarity and accountability across our Group.