


ANNEXURE A: OUR TRADEMARKS, BRAND NAMES AND OTHER INTELLECTUAL PROPERTY RIGHTS

Save as disclosed below, as at the LPD, we do not have any other patents, trademarks, brand names, technical assistance agreements, franchises and other intellectual property rights:

Trademarks

As at the LPD, we have the following trademarks:

Malaysia

No.	Trademark ⁽¹⁾	Registered owner	Registration no.	Place of registration	Expiry date	Class/ Description of trademark
1.		SkyeChip	TM2020003011	Malaysia	17 February 2030	9: Semiconductors (integrated circuits); simulation software; artificial intelligence software. 42: Engineering design services; software design; software development; software consultancy; software engineering.
2.		SkyeChip	TM2023014414	Malaysia	23 May 2033	9: Computer software for computer-aided design/computer-aided manufacturing (cad/cam). 42: Computer aided engineering design services; computer hardware design services; computer system design services; platform as a service (PaaS).

Note:

(1) Trademark 2 is in colour.

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Patents

As at the LPD, we have the following patents:

Malaysia

<u>No.</u>	<u>Title of invention</u>	<u>Registered owner / Applicant</u>	<u>Registration / Application no.</u>	<u>Place of registration</u>	<u>Date of grant / Filing date</u>
Registered patents					
1.	A memory controller system and a method for memory scheduling of a storage device	SkyeChip	MY-205208-A	Malaysia	7 October 2024
2.	A memory sequencer system and a method of memory sequencing using thereof	SkyeChip	MY-206628-A	Malaysia	27 December 2024
3.	A clocking system and a method of clock synchronisation	SkyeChip	MY-204260-A	Malaysia	19 August 2024
4.	A generic physical layer providing a unified architecture for interfacing with an external memory device and methods of interfacing with an external memory device	SkyeChip	MY-205100-A	Malaysia	2 October 2024
5.	A voltage clamping circuit for protecting an internal circuitry and a method of operating thereof	SkyeChip	MY-203723-A	Malaysia	16 July 2024
6.	An apparatus and a method for synchronising output clock signals across a plurality of phase-locked loops	SkyeChip	MY-205935-A	Malaysia	21 November 2024

ANNEXURE A: OUR TRADEMARKS, BRAND NAMES AND OTHER INTELLECTUAL PROPERTY RIGHTS (Cont'd)

No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
7.	An apparatus and a method for handling non-continuous data transfer for a decision feedback equalizer in a memory subsystem	SkyeChip	MY-208672-A	Malaysia	23 May 2025
8.	A memory controller for improving data integrity and providing data security and a method of operating thereof	SkyeChip	MY-210319-A	Malaysia	11 September 2025
Applications under review					
1.	A I/O transmitter circuitry for supporting multi-modes serialisation	SkyeChip	PI2021000907	Malaysia	19 February 2021
2.	A memory controller system and a method of pre-scheduling memory transaction for a storage device	SkyeChip	PI2021006393	Malaysia	25 October 2021
3.	A network-on-chip system for optimising data transfer	SkyeChip	PI2022004376	Malaysia	12 August 2022
4.	A method and a system for network-on-chip arbitration	SkyeChip	PI2022006385	Malaysia	11 November 2022
5.	A system and a method for aligning a programmable clock or strobe	SkyeChip	PI2022007112	Malaysia	14 December 2022
6.	Network-on-chip packetization and routing method and apparatus for scalable high-performance networking on and off chip	SkyeChip	PI2023001073	Malaysia	1 March 2023

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
7.	A system and a method for network-on-chip power management	SkyeChip	PI2023006579	Malaysia	25 October 2023
8.	A method of generating and assigning identifier information to each router in a network-on-chip for arbitrating a data packet	SkyeChip	PI2023006704	Malaysia	1 November 2023
9.	Offset calibration method and apparatus for high bandwidth memory 3 (HBM3)	SkyeChip	PI2023007402	Malaysia	5 December 2023
10.	Network-on-chip region-based routing table generation method	SkyeChip	PI2024000695	Malaysia	31 January 2024
11.	Feedforward regulated circuitry system and method for regulating power supply using thereof	SkyeChip	PI2024000736	Malaysia	2 February 2024
12.	Circuitry system and method for regulating voltage thereof using dynamic decoupling capacitor	SkyeChip	PI2024002016	Malaysia	3 April 2024
13.	A digital delay line of a memory system and method of adjusting timing of clocks using thereof	SkyeChip	PI2024000530	Malaysia	24 January 2024
14.	A coherent system and a method of maintaining cache coherence using thereof	SkyeChip	PI2024000899	Malaysia	8 February 2024
15.	Circuitry for low-dropout regulator with overvoltage protection circuit	SkyeChip	PI2024001998	Malaysia	2 April 2024

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
16.	Computer-implemented system and method for electronic systems design synchronization	SkyeChip	PI2024002238	Malaysia	18 April 2024
17.	Method and apparatus of receive enable margining in memory interface	SkyeChip	PI2022000379	Malaysia	20 January 2022
18.	Method of debugging network-on-chip	SkyeChip	PI2022004591	Malaysia	24 August 2022
19.	System and method for transferring configuration, management, debug information and asynchronous events between network-on-chip (NOC) and external interface	SkyeChip	PI2022005661	Malaysia	12 October 2022
20.	Feedforward circuitry system for direct AC-coupling and method for regulating voltage using thereof	SkyeChip	PI2024004618	Malaysia	8 August 2024
21.	Instantiatable and stampable partitions for network-on-chip architecture and method of processing data using thereof	SkyeChip	PI2024004892	Malaysia	22 August 2024
22.	Read transactions management in a memory controller	SkyeChip	PI2025001434	Malaysia	4 March 2025
23.	Command buffer for a memory controller	SkyeChip	PI2025001435	Malaysia	4 March 2025
24.	A method for forwarding and returning packets in a multi-die system-on-chip (SOC)	SkyeChip	PI2025002128	Malaysia	8 April 2025

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
25.	Method and system for routing packets across multiple dies using orientation aware hierarchical identification (ID)	SkyeChip	PI2025002874	Malaysia	9 May 2025
26.	Method and apparatus for network on chips (NOCS) tunnelling over universal chiplet in interconnect express (UCIE) flit format	SkyeChip	PI2025002873	Malaysia	9 May 2025
27.	Method for performing multicast transaction in a network-on-chip and the system thereof	SkyeChip	PI2025004182	Malaysia	10 July 2025
28.	A computer implemented system and method for managing electronic circuit designs through grouping of design units and creation and reuse of stamp templates	SkyeChip	PI2025004957	Malaysia	14 August 2025

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China

No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
Registered Patents					
1.	A memory controller system and a method for memory scheduling of a storage device	SkyeChip	CN 114281723 B	China	26 November 2024
2.	A clocking system and a method of clock synchronisation	SkyeChip	CN 114647598 B	China	30 August 2024
3.	A generic physical layer providing a unified architecture for interfacing with an external memory device and methods of interfacing with an external memory device	SkyeChip	CN 114691556 B	China	16 July 2024
4.	A voltage clamping circuit for protecting an internal circuitry and a method of operating thereof	SkyeChip	CN 114690825 B	China	30 January 2024
5.	A I/O transmitter circuitry for supporting multi-modes serialisation	SkyeChip	CN 114978202 B	China	26 March 2024
6.	An apparatus and a method for handling non-continuous data transfer for a decision feedback equalizer	SkyeChip	CN 115116503 B	China	31 December 2024
7.	A memory controller for improving data integrity and a method of operating thereof	SkyeChip	CN 114880160 B	China	24 June 2025
Applications under review					
1.	A memory sequencer system and a method of memory sequencing using thereof	SkyeChip	202110058327.4	China	16 January 2021

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
2.	An apparatus and a method for synchronising output clock signals across a plurality of phase-locked loops	SkyeChip	202210009515.2	China	5 January 2022
3.	A memory controller system and a method of pre-scheduling memory transaction for a storage device	SkyeChip	202210089363.1	China	25 January 2022
4.	A network-on-chip system for optimising data transfer	SkyeChip	202211285979.2	China	20 October 2022
5.	A method and a system for network-on-chip arbitration	SkyeChip	202310092934.1	China	3 February 2023
6.	A system and a method for aligning a programmable clock or strobe	SkyeChip	202310189266.4	China	23 February 2023
7.	Network-on-chip packetisation and routing method and apparatus for scalable high-performance networking on and off chip	SkyeChip	202310573036.8	China	19 May 2023
8.	A system and a method for network-on-chip power management	SkyeChip	202410059453.5	China	16 January 2024
9.	A method of generating and assigning identifier information to each router in a network on-chip for arbitrating a data packet	SkyeChip	202410030591.0	China	8 January 2024
10.	Offset calibration method and apparatus for high bandwidth memory 3 (HBM3)	SkyeChip	202410329118.2	China	21 March 2024

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
11.	Network-on-chip region-based routing table generation method	SkyeChip	202410645999.9	China	23 May 2024
12.	Feedforward regulated circuitry system and method for regulating power supply using thereof	SkyeChip	202410499863.1	China	24 April 2024
13.	A coherent system and a method of maintaining cache coherence using thereof	SkyeChip	202410556664.X	China	7 May 2024
14.	Method and apparatus of receive enable margining in memory interface	SkyeChip	202210552248.3	China	20 May 2022
15.	Method of debugging network-on-chip	SkyeChip	202211255356.0	China	13 October 2022
16.	System and method for transferring configuration, management, debug information and asynchronous events between network-on-chip (NOC) and external interface	SkyeChip	202310127110.3	China	16 February 2023
17.	A digital delay line of a memory system and method of adjusting timing of clocks using thereof	SkyeChip	202410973925.8	China	19 July 2024
18.	Circuitry for low-dropout regulator with overvoltage protection circuit	SkyeChip	202410991670.8	China	23 July 2024
19.	Computer-implemented system and method for electronic systems design synchronisation	SkyeChip	202410958482.5	China	17 July 2024

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
20.	Circuitry system and method for regulating voltage thereof using dynamic decoupling capacitor	SkyeChip	202411568218.7	China	5 November 2024
21.	Instantiatable and stampable partitions for network-on-chip architecture and method of processing data using thereof	SkyeChip	202510174896.3	China	18 February 2025
22.	Feedforward circuitry system for direct AC-coupling and method for regulating voltage using thereof	SkyeChip	202510276336.9	China	10 March 2025
23.	Read transactions management in a memory controller	SkyeChip	202510509517.1	China	22 April 2025
24.	Command buffer for a memory controller	SkyeChip	202510509379.7	China	22 April 2025

Note:

As at the LPD, there are 5 patents pending application for registration in China.

ANNEXURE A: OUR TRADEMARKS, BRAND NAMES AND OTHER INTELLECTUAL PROPERTY RIGHTS (Cont'd)**USA**

No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
Registered patents					
1.	Memory controller system and a method for memory scheduling of a storage device	SkyeChip	11,609,709 B2	USA	21 March 2023
2.	Memory sequencer system and a method of memory sequencing using thereof	SkyeChip	11,442,878 B2	USA	13 September 2022
3.	Clocking system and a method of clock synchronisation	SkyeChip	11,575,383 B2	USA	7 February 2023
4.	Generic physical layer providing a unified architecture for interfacing with an external memory device and methods of interfacing with an external memory device	SkyeChip	11,373,694 B1	USA	28 June 2022
5.	Voltage clamping circuit for protecting an internal circuitry and a method of operating thereof	SkyeChip	11,411,394 B2	USA	9 August 2022
6.	Memory controller for improving data integrity and providing data security and a method of operating thereof	SkyeChip	12,210,633 B2	USA	28 January 2025
7.	I/O transmitter circuitry for supporting multi-modes serialisation	SkyeChip	11,349,481 B1	USA	31 May 2022
8.	Apparatus and a method for handling non-continuous data transfer for a decision feedback equalizer in a memory subsystem	SkyeChip	11,349,691 B1	USA	31 May 2022

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
9.	Apparatus and a method for synchronising output clock signals across a plurality of phase-locked loops	SkyeChip	11,509,312 B1	USA	22 November 2022
10.	Memory controller system and a method of pre-scheduling memory transaction for a storage device	SkyeChip	11,829,643 B2	USA	28 November 2023
11.	Method and a system for network-on-chip arbitration	SkyeChip	12,199,884 B2	USA	14 January 2025
12.	Method and apparatus of receive enable margining in memory interface	SkyeChip	12,125,518 B2	USA	22 October 2024
13.	System and method for transferring configuration, management, debug information and asynchronous events between network-on-chip (NOC) and external interface	SkyeChip	12,149,407 B2	USA	19 November 2024
14.	A network-on-chip system for optimising data transfer	SkyeChip	12,380,056 B2	USA	5 August 2025
Applications under review					
1.	System and a method for aligning a programmable clock or strobe	SkyeChip	18/170,599	USA	17 February 2023
2.	Network-on-chip packetisation and routing method and apparatus for scalable high-performance networking on and off chip	SkyeChip	18/335,062	USA	14 June 2023

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
3.	System and a method for network-on-chip power management	SkyeChip	18/399,978	USA	29 December 2023
4.	Method of generating and assigning identifier information to each router in a network on-chip for arbitrating a data packet	SkyeChip	18/417,849	USA	19 January 2024
5.	Offset calibration method and apparatus for high bandwidth memory 3 (HBM3)	SkyeChip	18/423,817	USA	26 January 2024
6.	Circuitry system and method for regulating voltage thereof using dynamic decoupling capacitor	SkyeChip	18/737,958	USA	8 June 2024
7.	Method of debugging network-on-chip	SkyeChip	17/938,810	USA	7 October 2022
8.	Feedforward regulated circuitry system and method for regulating power supply using thereof	SkyeChip	18/814,902	USA	26 August 2024
9.	Coherent system and a method of maintaining cache coherence using thereof	SkyeChip	18/885,842	USA	16 September 2024
10.	Network-on-chip region-based routing table generation method	SkyeChip	18/787,936	USA	29 July 2024
11.	Adigital delay line of a memory system and method of adjusting timing of clocks using thereof	SkyeChip	18/887,293	USA	17 September 2024
12.	Circuitry for low-dropout regulator with overvoltage protection circuit	SkyeChip	18/888,779	USA	18 September 2024

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No.	Title of invention	Registered owner / Applicant	Registration / Application no.	Place of registration	Date of grant / Filing date
13.	Computer-implemented system and method for electronic systems design synchronisation	SkyeChip	18/891,668	USA	20 September 2024
14.	Feedforward circuitry system for direct AC-coupling and method for regulating voltage using thereof	SkyeChip	19/070,683	USA	5 March 2025
15.	Read transactions management in a memory controller	SkyeChip	19/077,141	USA	12 March 2025
16.	Command buffer for a memory controller	SkyeChip	19/174,133	USA	9 April 2025
17.	Instantiatable and stampable partitions for network-on-chip architecture and method of processing data using thereof	SkyeChip	19/203,044	USA	8 May 2025

Note:

As at the LPD, there are 5 patents pending application for registration in the USA.